NCR 53C710

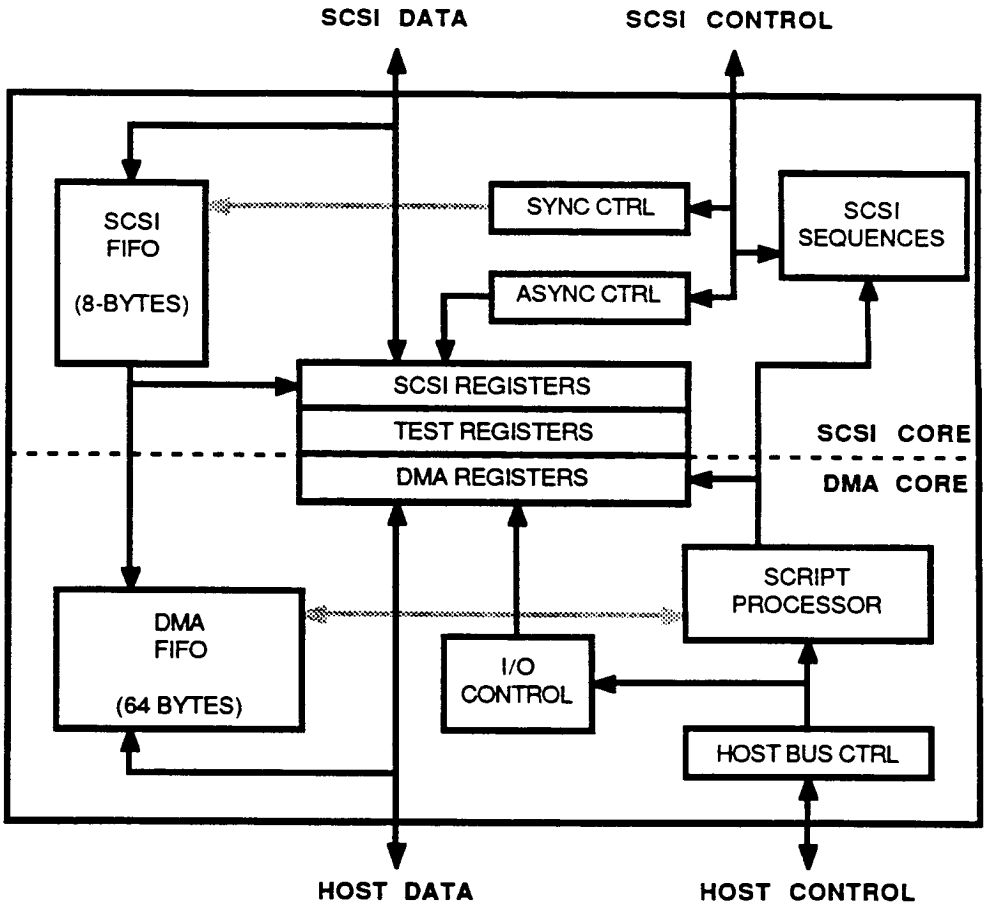
Features

- 10.0 MBytes/sec Fast SCSI-2
- 66 MBytes/sec 32-Bit Host Bus DMA Bandwidth @ 33 MHz
- Enhanced SCRIPT Capabilities:
  - Relative Jump
  - Table Indirect Data Mode
  - Read/Write System Memory
  - Read/Write Registers
  - Arithmetic Operations
  - Memory-to-Memory DMA Transfers
- Big or Little Endian Byte Ordering
- SCSI Byte-to-Byte Activity Timer
- Register Parity during Slave Reads
- Glitchless SCSI on Power Up/Down

General Description

The NCR 53C710 is the second member of the 53C700 family of intelligent, single-chip, third generation SCSI host adapters. A high performance SCSI core and an intelligent 32-bit bus master DMA core are integrated with a SCSI SCRIPTs Processor to accommodate the flexibility requirements of not only SCSI-1 and SCSI-2, but future SCSI standards as well. This flexibility is supported while solving the protocol overhead problems that have plagued all previous intelligent and non-intelligent adapter designs.

Figure 1. 53C710 Block Diagram



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SIGNAL DESCRIPTIONS

The 53C710 host bus can operate in one of two modes: Asynchronous, Synchronous. The bus mode is selected with the BS pin. A slash ("/") indicates an active low signal. See the DC Specifications section for specific pin type (three-state, open drain, etc.) and current drive capabilities.

Table 1. Interface Signals

Name		Type		
Async	**Sync**	**Slave**	**Mstr**	**Description**
D(31:0)	D(31:0)	I/O	I/O	Host Data Bus Main 32-bit data path into host memory.
DP(3:0)	DP(3:0)	I/O	I/O	Host Bus Data Parity DP0 provides parity for D(7:0), DP1 for D(15:8), etc. Parity is valid on all byte lanes, including unused lanes. When the parity through mode is disabled, DP3 becomes a hardware abort input (ABRT/).
DS/	DLE			Data Strobe-Data Latch Enable
		Z	I/O	DS/ Indicates that valid data has been or should be placed on the data lines.
		I	I	DLE Data Latch Enable transparently latches read data into the 53C710 when in Sync.
A(31:0)	A(31:0)	I	O	Address Bus Provides an address bus to the host memory.
AS/	TS/	I	O	Address Strobe -Transfer Start AS/ Indicates that a valid address is on A(31:0). TS/ Transfer Start indicates that a bus cycle is starting and all of the status and address lines are valid.
R_W/	R_W/	I	O	Read-Write Indicates the direction of the data transfer relative to the current master
SIZ(1:0)	SIZ(1:0)	I	O	Transfer Size Indicates the current transfer size. 00 Long word (4 bytes) 01 Byte (1 byte) 10 Word (2 bytes, not supported in slave mode) 11 Async: Illegal Sync: Cache-Line Burst
STERM/	TA/	I/O	I	Synchronous Cycle Termination-Transfer Acknowledge STERM/ Acknowledges transfer to a 32-bit wide port TA/ Acknowledges transfer to a 32-bit wide port

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Table 1. Interface Signals (continued)

Name		Type		
Async	Sync	Slave	Mstr	Description
BERR/	TEA/	I/O	I	Bus Error Acknowledge-Transfer Error Acknowledge BERR/ Indicates that a bus fault has occurred. Used with HALT/ to force a bus retry. TEA/ Indicates that a bus fault has occurred.
HALT/	TIP/	Z	I/O	Halt-Transfer in progress HALT/ Input ONLY, used with BERR/ to indicate a bus retry cycle. TIP/ Bidirectional, indicates that bus activity is in progress.
SLACK/	SLACK/	O	O	Slave Acknowledge Asserted to indicate the internal end of a slave mode cycle. The external slave cycle ends when the 53C710 observes either STERM/-TA/ or BERR/ -TEA/.
FC(2:0)	FC(2:0)	Z	O	Function Codes Indicates the status of the current bus cycle. FC0=1 Indicates data space; it is the default for all transfers FC0=0 Indicates program space. It may be optionally selected when setting the PD bit. FC1 User definable from register bits. FC2 User definable from register bits.
SC(1:0)	SC(1:0)	Z (O)	O	Snoop Control Indicates the bus snooping level. The bits are user programmable through register bits. They are asserted when the 53C710 is the bus master (SC(1:0) may optionally be used as pure outputs, active in both master and slave modes).
MASTER/	MASTER/	O	O	Master Status Driven low when the 53C710 becomes bus master.
FETCH/	FETCH/	O	O	Fetching Op Code Indicates that the next bus request will be for an op code fetch.
BR/	BR/	O	O	Bus Request Indicates that there is a request to use the host bus.
BG/	BG/	I	I	Bus Grant Indicates that the host bus has been granted to the 53C710.
BGACK/	BB/	Z	I/O	Bus Grant Acknowledge-Bus Busy (can be wire-OR'ed) BGACK/ Indicates that the 53C710 or another device has taken control of the host bus signals. BB/ Indicates that the 53C710 or another device has taken control of the host bus signals.

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Table 1. Interface Signals (continued)

Name		Type		
Async	Sync	Slave	Mstr	Description
BOFF/	BOFF/	I	I	Back off Forces the 53C710 to relinquish bus mastership at the end of the current cycle, if the proper setup timing requirements are met. The cycles will be resumed when BOFF/ is deasserted.
BCLK	BCLK	I	I	Bus Clock This clock controls all host related activity.
RESET/	RESET/	I	I	Chip Reset Forces a full chip reset.
CS/	CS/	I	I	Chip Select Selects the 53C710 as a slave I/O device. When CS/ is detected: Async: CBACK/ is deasserted Sync: TBI/ is asserted.
IRQ/	IRQ/	O	O	Interrupt Indicates that service is required from the host CPU.
UPSO	TT0/	Z	O	User Programmable Status-Transfer Type Zero UPSO: General purpose line. The value in a register bit is asserted while the chip is a bus master. TT0/: Indicates the current bus transfer type. This bit can be programmed from a register bit (default = 0). It is asserted only when the 53C710 is bus master.
CBREQ/	TT1/	Z	O	Cache Burst Request-Transfer type bit 1 CBREQ/: Cache Burst Request indicates an attempt to execute a line transfer of four long words TT1/: Transfer Type bit 1, three-state output line indicating the current bus transfer type. This bit can be programmed from a register bit (default = 0). It is only asserted when the 53C710 is bus master.
CBACK/	TBI/	O	I	Cache Burst Acknowledge-Transfer Burst Inhibit CBACK/: Indicates that the memory system or 53C710 can handle a burst request. In slave mode this signal is deasserted in response to CS/. TBI/: Transfer Burst Inhibit indicates that the memory or the 53C710 can not handle a burst request at this time. In slave mode this signal is asserted in response to CS/.
BS	BS	I	I	Bus Mode Select Selects between asynchronous and synchronous host bus modes. BS=0: Synchronous (68040-like) host bus mode BS=1: Asynchronous (68030-like) host bus mode

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Table 1. Interface Signals (continued)

Name		Type		
Async	Sync	Slave	Mstr	Description
BIG_LIT/	BIG_LIT/	I	I	Big/Little Endian Select Selects the byte order interpretation of data transferred between the HOST and SCSI bus. It also affects how the register set is addressed. BIG_LIT/=0 Little endian byte order BIG_LIT/=1 Big endian byte order
SCLK	SCLK	I	I	SCSI Clock SCLK is used to derive all SCSI related timings. The speed of this clock will be determined by the application's requirements; in some applications SCLK and BCLK may be tied to the same source.
SDATA/	SDATA/	I/O	I/O	SCSI Data SD/(7:0) 8 bit SCSI data bus SDBP/ SCSI Data parity bit
SCTRL/	SCTRL/	I/O	I/O	SCSI Control CD/ SCSI phase line, command/data IO/ SCSI phase line, input/output MSG/ SCSI phase line, message REQ/ Data handshake signal from target device ACK/ Data handshake signal from initiator device BSY/ SCSI bus arbitration signal, signal busy SEL/ SCSI bus arbitration signal, select device ATN/ Attention, the initiator is requesting a message in phase. RST/ SCSI bus reset.
SDIR(7:0)	SDIR(7:0)	O	O	Differential support lines Driver direction control for SCSI data lines.
SDIRP	SDIRP	O	O	Differential support line Driver direction control for SCSI parity signal.
BSYDIR	BSYDIR	O	O	Differential support line Driver enable control for SCSI BSY/ signal.
SELDIR	SELDIR	O	O	Differential support line Driver enable control for SCSI SEL/ signal.
RSTDIR	RSTDIR	O	O	Differential support line Driver enable control for SCSI RST/ signal.
IGS	IGS	O	O	Differential support line Direction control for initiator driver group.
TGS	TGS	O	O	Differential support lines Direction control for target driver group.

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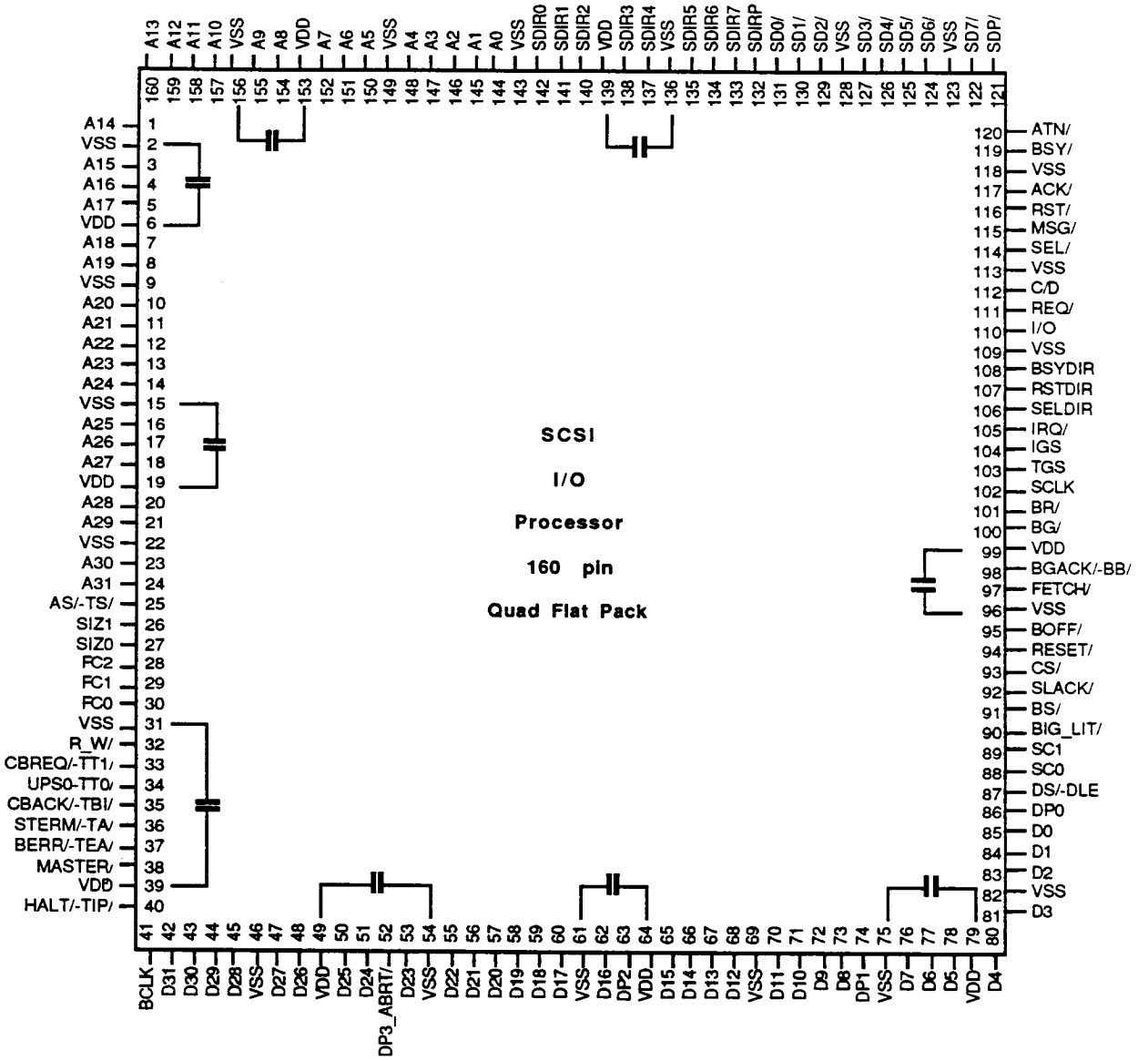
Figure 2. 53C710 Pinout



NOTE: The above decoupling capacitor arrangement shown is recommended to maximize the benefits of the internal split ground system. Capacitor values between 0.01 and 0.1 µF should provide adequate noise isolation. Because of the number of high current drivers on the 53C710, a multi-layer PC board with power & ground planes is required.

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REGISTER DESCRIPTIONS

This section contains descriptions of all 53C710 registers. Table 2, below, summarizes the 53C710 register set. Figure 3, on the following page, shows a more graphical representation of the register set and lists registers by both their big and little endian addresses.

Table 2. Register Addresses and Descriptions

Address (Hex)	Read/Write	Label	Description
00	R/W	SCNTL0	SCSI Control Register 0
01	R/W	SCNTL1	SCSI Control Register 1
02	R/W	SDID	SCSI Destination ID Register
03	R/W	SIEN	SCSI Interrupt Enable Register
04	R/W	SCID	SCSI Chip ID Register
05	R/W	SXFER	SCSI Transfer Register
06	R/W	SODL	SCSI Output Data Latch Register
07	R/W	SOCL	SCSI Output Control Latch Register
08	R/W	SFBR	SCSI First Byte Received Register
09	R	SIDL	SCSI Input Data Latch Register
0A	R	SBDL	SCSI Bus Data Lines Register
0B	R/W	SBCL	SCSI Bus Control Lines Register
0C	R	DSTAT	DMA Status Register
0D	R	SSTAT0	SCSI Status Register 0
0E	R	SSTAT1	SCSI Status Register 1
0F	R	SSTAT2	SCSI Status Register 2
10-13	R/W	DSA	Data Structure Address
14	R/W	CTEST0	Chip Test Register 0
15	R	CTEST1	Chip Test Register 1
16	R	CTEST2	Chip Test Register 2
17	R	CTEST3	Chip Test Register 3
18	R/W	CTEST4	Chip Test Register 4
19	R/W	CTEST5	Chip Test Register 5
1A	R/W	CTEST6	Chip Test Register 6
1B	R/W	CTEST7	Chip Test Register 7
1C-1F	R/W	TEMP	Temporary Stack Register
20	R/W	DFIFO	DMA FIFO Register
21	R/W	ISTAT	Interrupt Status Register
22	R/W	CTEST8	Chip Test Register 8
23	R/W	LCRC	Longitudinal Parity Register
24-26	R/W	DBC	DMA Byte Count Register
27	R/W	DCMD	DMA Command Register
28-2B	R/W	DNAD	DMA Next Address for Data Register
2C-2F	R/W	DSP	DMA SCRIPTs Pointer Register
30-33	R/W	DSPS	DMA SCRIPTs Pointer Save Register
34-37	R/W	SCRATCH	General Purpose Scratch Pad Register
38	R/W	DMODE	DMA Mode Register
39	R/W	DIEN	DMA Interrupt Enable Register
3A	R/W	DWT	DMA Watchdog Timer Register
3B	R/W	DCNTL	DMA Control Register
3C-3F	R	ADDER	Sum Output of Internal Adder

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Figure 3. 53C710 Register Address Map

Big Endian Mode					SCRIPTs Mode and Little Endian Mode
00	SIEN	SDID	SCNTL1	SCNTL0	00
04	SOCL	SODL	SXFER	SCID	04
08	SBCL	SBDL	SIDL	SFBR	08
0C	SSTAT2	SSTAT1	SSTAT0	DSTAT	0C
10	DSA				10
14	CTEST3	CTEST2	CTEST1	CTEST0	14
18	CTEST7	CTEST6	CTEST5	CTEST4	18
1C	TEMP				1C
20	LCRC	CTEST8	ISTAT	DFIFO	20
24	DCMD	DBC			24
28	DNAD				28
2C	DSP				2C
30	DSPS				30
34	SCRATCH				34
38	DCNTL	DWT	DIEN	DMODE	38
3C	ADDER				3C

Notes

- Throughout this document, registers are referenced by their little endian addresses. See Figure 3 (above) for big endian addresses.
- The term "set" is used to refer to bits that are programmed to a binary one. Similarly, the terms "clear" and "reset" are used to refer to bits that are programmed to a binary zero.
- Reserved bits are designated as "RES" in each register map. These bits should always be written to zero; mask all information read from them.
- Unless otherwise indicated, all bits in registers are active high, ie. the feature is enabled by setting the bit.
- The bottom line of every register diagram shows the default. Default refers to the register values after the chip is powered-up or reset.
- Registers can be addressed as bytes or long words only; other access sizes result in bus errors.
- The only register that the host CPU can access while the 53C710 is executing SCRIPTs is the ISTAT register; attempts to access other registers will interfere in the operation of the chip. All registers are accessible via SCRIPTs, however.

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Register 00 SCSI Control Zero — Read/Write (SCNTL0)

7	6	5	4	3	2	1	0
ARB1	ARB0	START	WATN/	EPC	EPG	AAP	TRG
1	1	0	0	0	0	0	0

Bit 7-6 ARB(1:0) - Arbitration Mode

ARB1	ARB0	Arbitration Mode
0	0	Simple Arbitration
0	1	Reserved
1	0	Reserved
1	1	Full Arbitration,Selection or Reselection

Simple Arbitration

1) The 53C710 waits for a bus free condition to occur.

2) It asserts BSY/ and its SCSI ID (contained in the SCID register) onto the SCSI bus

   If the SEL/ signal is asserted by another SCSI device, the 53C710 will deassert BSY/, deassert its ID and set the Lost Arbitration bit in the SSTAT1 register.

3) After an arbitration delay, the CPU should read the SBDL register to check if a higher priority SCSI ID is present. If no higher priority ID bit is set, and the Lost Arbitration bit is not set, the 53C710 has won arbitration.

4) Once the 53C710 has won arbitration, SEL must be asserted via the SOCL for a bus clear plus a bus settle delay (1.2 µS) before a low level selection can be performed.

Full Arbitration, Selection/Reselection

1) The 53C710 waits for a bus free condition.

2) It asserts BSY/ and its SCSI ID (the highest priority ID stored in the SCID register) onto the SCSI bus.

3) If the SEL/ signal is asserted by another SCSI device or if the 53C710 detects a higher priority ID, the 53C710 will deassert BSY/, deassert its ID, and wait until the next bus free state to try arbitration again.

4) The 53C710 repeats arbitration until it wins control of the SCSI bus. When it has won, the Won Arbitration Bit is set in the SSTAT1 register.

5) The 53C710 performs selection by asserting the following onto the SCSI bus: SEL/, the target's ID (stored in the SDID register) and the 53C710's ID (the highest priority ID stored in the SCID register).

6) After a selection is complete, the Function Complete bit is set in the SSTAT0 register.

7) If a selection timeout occurs, the Selection Timeout bit is set in the SSTAT0 register.

Bit 5 START - Start Sequence

When this bit is set, the 53C710 will start the arbitration sequence indicated by the Arbitration Mode bits. The Start Sequence bit is used in low level mode; when executing SCSI SCRIPTs, this bit is controlled by the SCRIPTs processor. An arbitration sequence should not be started if the connected bit in the SCNTL1 register indicates that 53C710 is already connected to the SCSI bus.

This bit is automatically cleared when the arbitration sequence is complete. An arbitration sequence can be aborted by clearing this bit. If a sequence is aborted, the connected bit in the SCNTL1 register should be checked to verify that the 53C710 did not connect to the SCSI bus.

Bit 4 WATN - Select with ATN/ on a Start Sequence

When this bit is set, the SCSI ATN/ signal will be asserted during the selection phase (ATN/ is asserted at the same time BSY/ is deasserted while selecting a target). If a selection timeout occurs while attempting to select a target device, ATN/ will be deasserted at the same time SEL/ is deasserted.

When this bit is clear, the ATN/ signal will not be asserted during selection.

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When executing SCSI SCRIPTs, this bit is controlled by the SCRIPTs Processor, but it may be set manually in low level mode.

Bit 3 EPC - Enable Parity Checking

When this bit is set, the SCSI data bus is checked for odd parity when data is received from the SCSI bus in either initiator or target mode. The host data bus is checked for odd parity if bit 2, the Enable Parity Generation bit, is cleared. Host data bus parity is checked as data is loaded into the SODL register when sending SCSI data in either initiator or target mode. If a parity error is detected, bit 0 of the SSTAT0 register is set and an interrupt may be generated.

If the 53C710 is operating in target mode, bytes with parity errors written into the DMA FIFO can be prevented from being written to the SCSI bus. A phase change to Message In phase must be generated to indicate this condition.

If the 53C710 is operating in initiator mode and a parity error is detected, ATN/ can optionally be asserted, but the transfer continues until the target changes phase to Message Out.

When this bit is cleared, parity errors are not reported.

Bit 2 EPG - Enable Parity Generation/Parity Through

When this bit is set, the SCSI parity bit will be generated by the 53C710. The host data bus parity lines DP(3:0) are ignored and should not be used as parity signals. When this bit is cleared, the parity present on the host data parity lines will flow through the 53C710's internal FIFOs and be driven onto the SCSI bus when sending data (if the host bus is set to even parity, it is changed to odd before it is sent to the SCSI bus).

This bit is set to enable the DP3_ABRT/ pin to function as an abort input (ABRT/).

Bit 1 AAP - Assert ATN/ on Parity Error

When this bit is set, the 53C710 automatically asserts the SCSI ATN/ signal upon detection of a parity error. ATN/ is only asserted in initiator mode. The ATN/ signal is asserted before deasserting ACK/ during the byte transfer with the parity error. The Enable Parity Checking bit must also be set for the 53C710 to assert ATN/ in this manner. The following parity errors can occur:

1) A parity error detected on data received from the SCSI bus.

2) A parity error detected on data transferred to the 53C710 from the host data bus.

If the Assert ATN/ on Parity Error bit is cleared or the Enable Parity Checking bit is cleared, ATN/ will not be automatically asserted on the SCSI bus when a parity error is received.

Bit 0 TRG - Target Mode

This bit determines the default operating mode of the 53C710, though there are instances when the chip may act in a role other than the default. For example, a mostly-initiator device may be selected as a target. An automatic mode change does affect the state of this bit. After completion of a mode change I/O operation, the 53C710 returns to the role defined by this bit.

When this bit is set, the chip is a target device by default. When the target mode bit is cleared, the 53C710 is an initiator device by default.

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Register 01 SCSI Control One — Read/Write (SCNTL1)

EXC	ADB	ESR	CON	RST	AESP	SND	RCV
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0

Bit 7 EXC - Extra Clock Cycle of Data Setup

When this bit is set, an extra clock period of data setup is added to each SCSI data transfer. The extra data setup time can provide additional system design margin, though it will affect the SCSI transfer rates. Clearing this bit disables the extra clock cycle of data setup time.

Bit 6 ADB - Assert SCSI data bus

When this bit is set, the 53C710 drives the contents of the SCSI Output Data Register (SODL) onto the SCSI data bus. When the 53C710 is an initiator, the SCSI I/O signal must be inactive to assert the SODL contents onto the SCSI bus. When the 53C710 is a target, the SCSI I/O signal must be active for the SODL contents to be asserted onto the SCSI bus. The contents of the SODL register can be asserted at any time, even before the 53C710 is connected to the SCSI bus. This bit should be cleared when executing SCSI SCRIPTs. It is normally used only for diagnostics testing or operation in low level mode.

Bit 5 ESR - Enable Selection & Reselection

When this bit is set, the 53C710 will respond to bus-initiated selections and reselections. The 53C710 can respond to selections and reselections in both initiator and target roles. If the disconnect/reconnect feature is to be supported, this bit should be set as part of the initialization routine.

Bit 4 CON - Connected

This bit is automatically set anytime the 53C710 is connected to the SCSI bus as an initiator or as a target. It will be set after successfully completing arbitration or when the 53C710 has responded to a bus-initiated selection or reselection. It will also be set after successfully completing simple arbitration when operating in low level mode. When this bit is clear, the 53C710 is not connected to the SCSI bus.

The CPU can force a connected or disconnected condition by setting or clearing this bit. This feature would be used primarily during loopback mode.

Bit 3 RST - Assert SCSI RST/ signal

Setting this bit asserts the SCSI RST/ signal. The RST/ output remains asserted until this bit is cleared. The 25 µsec minimum assertion time defined in the SCSI specification must be timed out by the controlling microprocessor or a SCRIPT loop.

Bit 2 AESP - Assert even SCSI Parity (force bad parity)

When this bit is set and the Enable Parity Generation bit is set in the SCNTL0 register, the 53C710 asserts even parity. It forces a SCSI parity error on each byte sent to the SCSI bus from the 53C710. If parity checking is enabled, then the 53C710 checks data received for even parity. This bit is used for diagnostic testing and should be clear for normal operation. It can be used to generate parity errors to test error handling functions.

Bit 1 SND - Start SCSI Send Operation

Setting this bit initiates a SCSI send operation. It is automatically set by the SCRIPTs PROCESSOR to start a SCSI send operation when executing SCSI SCRIPTs. It is intended for low level operation.

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Bit 0 RCV - Start SCSI Receive Operation

Setting this bit initiates a SCSI receive operation. It is automatically set by the SCRIPTs PROCESSOR to start a SCSI receive operation when executing SCSI SCRIPTs. It may be set directly for low level operation.

Register 02 SCSI Destination ID (SDID) Read/Write

7	6	5	4	3	2	1	0
ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
0	0	0	0	0	0	0	0

Bits 7-0 ID(7:0) - SCSI ID

This register sets the SCSI ID of the device to be selected when executing a select or reselect command. Only one of these bits should be set for proper selection or reselection. When executing SCSI SCRIPTs, the SCRIPTs PROCESSOR writes the destination SCSI ID to this register. The SCSI ID is defined by the user in a SCSI SCRIPTs select or reselect instruction.

Note: When using Table Indirect I/O commands, the destination ID will be loaded from the data structure.

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Register 03 SCSI Interrupt Enable (SIEN) — Read/Write

7	6	5	4	3	2	1	0
M/A	FCMP	STO	SEL	SGE	UDC	RST/	PAR
0	0	0	0	0	0	0	0

Bit 7 — **M/A - Initiator Mode: Phase mismatch, or Target Mode: ATN/ active**

Bit 6 — **FCMP - Function Complete**

Bit 5 — **STO - SCSI Bus Timeout**

Bit 4 — **SEL - Selected or Reselected**

Bit 3 — **SGE - SCSI Gross Error**

Bit 2 — **UDC - Unexpected Disconnect**

Bit 1 — **RST/ - SCSI RST/ Received**

Bit 0 — **PAR - Parity Error**

This register contains the interrupt mask bits corresponding to the interrupting conditions described in the SSTAT0 register. Clearing a mask bit prevents IRQ/ from being asserted and ISTAT SIP from being set for the corresponding interrupt, but the status bit will still be set in the SSTAT0 register. Setting a mask bit enables the assertion of IRQ/ for the corresponding interrupt.

Register 04 SCSI Chip ID (SCID) — Read/Write

7	6	5	4	3	2	1	0
ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
0	0	0	0	0	0	0	0

Bits 7-0 ID(7:0) - SCSI ID

This register sets up the 53C710's SCSI ID. If more than one bit is set, the 53C710 will respond to each corresponding SCSI ID. The 53C710 always uses the highest priority SCSI ID during arbitration. For example, if an 84h were written to this register, the 53C710 would respond when another device selects ID 7 or ID 2. When arbitrating for the SCSI bus, ID 7 would be used as the 53C710's SCSI ID.

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Register 05 SCSI Transfer (SXFER) Read/Write

7	6	5	4	3	2	1	0
DHP	TP2	TP1	TP0	MO3	MO2	MO1	MO0
0	0	0	0	0	0	0	0

Note: When using Table Indirect I/O commands, bits 6-0 of this register will be loaded from the I/O data structure.

Bit 7 DHP - Initiator: Disable Halt on Parity Error, Target: Disable Halt on ATN/

In initiator mode, this bit is defined as Disable Halt on Parity Error. In target mode, this bit is defined as Disable Halt on Parity Error or ATN/.

When this bit is cleared, the 53C710 halts the SCSI data transfer when a parity error is detected or when the ATN/ signal is asserted. If ATN/ or a parity error is received in the middle of a data transfer, the 53C710 may transfer up to 3 additional bytes before halting to synchronize between internal core cells. During synchronous operation, the 53C710 transfers data until there are no outstanding synchronous offsets. If the 53C710 is receiving data, any data residing in the SCSI or DMA FIFOs is sent to memory before halting. While sending data in target mode with pass parity enabled, the byte with the parity error will not be sent across the SCSI bus.

When this bit is set, the 53C710 does not halt the SCSI transfer when ATN/ or a parity error is received.

Bits 6-4 TP(2:0) - SCSI Synchronous Transfer Period

These bits determine the SCSI synchronous transfer period used by the 53C710 when sending synchronous SCSI data in either initiator or target mode. The following table describes the possible combinations and their relationship to the synchronous data transfer period used by the 53C710.

TP2	TP1	TP0	XFERP
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

The actual Synchronous Transfer Period used by the 53C710 when transferring SCSI data is defined by the following equations:

The minimum synchronous transfer period when sending SCSI data:

PERIOD = TCP * (4 + XFERP + 1)

If Bit 7 in the SCNTL1 register is set (one extra clock cycle of data setup)

PERIOD = TCP * (4 + XFERP)

If Bit 7 in the SCNTL1 register is clear (no extra clock cycle of data setup)

The minimum synchronous transfer period when receiving SCSI data:

PERIOD = TCP * (4 + XFERP)

Whether sending or receiving, TCP = 1÷SCSI core clock frequency. The SCSI core clock frequency is determined by the CF(1:0) bits in the DCNTL register and SSCF(1:0) bits in SBCL.

The following table gives examples of synchronous transfer periods for SCSI-1 transfer rates.

CLK MHz	SCSI CLK ÷ DCNTL bits 7,6	XFERP	Sync XFER Period ns	Sync XFER Rate MBytes/ sec
50	÷2	0	160	6.25
50	÷2	1	200	5
40	÷2	0	200	5
37.50	÷1.5	0	160	6.25
33	÷1.5	0	181.82	5.5
25	÷1	0	160	6.25
20	÷1	0	200	5
16.67	÷1	0	239.95	4.17

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The table below gives example transfer periods for fast SCSI-2 transfer rates.

CLK MHz	SCSI CLK + SBCL bits 1,0	XFERP	Sync XFER Period ns	Sync XFER Rate MBytes/ sec
50	+1	0	80	12.5
50	+1	1	100	10.0
40	+1	0	100	10.0
37.50	+1	0	160.67	9.375
33	+1	0	121.21	8.25
25	+1	0	160	6.25
20	+1	0	200	5
16.67	+1	0	239.95	4.17

Bits 3-0 MO(3:0) - Maximum SCSI Synchronous Offset

MO3	MO2	MO1	MO0	Sync. Offset
0	0	0	0	Async. Operation
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	X	X	1	Reserved
1	X	1	X	Reserved
1	1	X	X	Reserved

These bits describe the maximum SCSI synchronous offset used by the 53C710 when transferring synchronous SCSI data in either initiator or target mode. The next table describes the possible combinations and their relationship to the synchronous data offset used by the 53C710. These bits determine the 53C710's method of transfer for Data In and Data Out phases only; all other information transfers will occur asynchronously.

Register 06 Read/Write SCSI Output Data Latch (SODL)

7	6	5	4	3	2	1	0
SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0
0	0	0	0	0	0	0	0

Bits 7-0 SD(7:0) - SCSI Output Data Latch

This register is used primarily for diagnostics testing or programmed I/O operation. Data written to this register is asserted onto the SCSI data bus by setting the Assert Data Bus bit in the SCNTL1 register. This register is used to send data via programmed I/O. Data flows through this register when sending data in any mode. It is also used to write to the synchronous data FIFO when testing the chip.

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Register 07 Read/Write
SCSI Output Control Latch (SOCL)

7	6	5	4	3	2	1	0
REQ	ACK	BSY	SEL	ATN	MSG	C/D	I/O
0	0	0	0	0	0	0	0

Bit 7 **REQ - Assert SCSI REQ/ signal**

Bit 6 **ACK - Assert SCSI ACK/ signal**

Bit 5 **BSY - Assert SCSI BSY/ signal**

Bit 4 **SEL - Assert SCSI SEL/ signal**

Bit 3 **ATN - Assert SCSI ATN/ signal**

Bit 2 **MSG - Assert SCSI MSG/ signal**

Bit 1 **C/D - Assert SCSI C/D signal**

Bit 0 **I/O - Assert SCSI I/O signal**

This register is used primarily for diagnostics testing or programmed I/O operation. It is controlled by the SCRIPTs PROCESSOR when executing SCSI SCRIPTs. SOCL should only be used when transferring data via programmed I/O. Some bits are set (1) or reset (0) when executing SCSI SCRIPTs. Do not write to the register once the 53C710 becomes connected and starts executing SCSI SCRIPTs.

Register 08 Read/Write
SCSI First Byte Received (SFBR)

7	6	5	4	3	2	1	0
1B7	1B6	1B5	1B4	1B3	1B2	1B1	1B0
0	0	0	0	0	0	0	0

Bits 7-0 1B(7:0) - First Byte Received

This register contains the first byte received in any asynchronous information transfer phase. For example, when the 53C710 is operating in initiator mode, this register contains the first byte received in Message In, Status phase, Reserved In and Data In.

When a Block Move Instruction is executed for a particular phase, the first byte received is stored in this register - even if the present phase is the same as the last phase. The first byte-received value for a particular input phase is not valid until after a MOVE instruction is executed.

This register is also the accumulator for register read-modify-writes with the SFBR as the destination. This allows bit testing after an operation.

Additionally, the SFBR register may be used to contain the device ID after a selection or reselection, if the COM bit is clear in the DCNTL register. However, for maximum flexibility it is strongly recommended that the ID byte be directed only to the LCRC register (COM bit set).

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Register 09 Read Only
SCSI Input Data Latch (SIDL)

7	6	5	4	3	2	1	0
SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0
0	0	0	0	0	0	0	0

Bits 7-0 SD(7:0) - SCSI Input Data Latch

This register is used primarily for diagnostics testing, programmed I/O operation or error recovery. Data received from the SCSI bus can be read from this register. Data can be written to the SODL register and then read back into the 53C710 by reading this register to provide "loopback" testing. When receiving SCSI data, the data will flow into this register and out to the host FIFO. This register differs from the SBDL register, this register contains latched data and the SBDL always contains exactly what is currently on the SCSI data bus.

Register 0A Read Only
SCSI Bus Data Lines (SBDL)

7	6	5	4	3	2	1	0
DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
X	X	X	X	X	X	X	X

Bits 7-0 SD(7:0) - SCSI Bus Data

This register contains the SCSI data bus status. Even though the SCSI data bus is active low, these bits are active high. The signal status is not latched and is a true representation of exactly what is on the data bus at the time that the register is read. This register is used when receiving data via programmed I/O. This register can also be used for diagnostics testing or in low level mode.

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Register 0B Read/Write
SCSI Bus Control Lines (SBCL)

7	6	5	4	3	2	1	0
REQ	ACK	BSY	SEL	ATN	MSG	C/D	I/O
X	X	X	X	X	X	X	X

Bit 7 **REQ - REQ/ status**

Bit 6 **ACK - ACK/ status**

Bit 5 **BSY - BSY/ status**

Bit 4 **SEL - SEL/ status**

Bit 3 **ATN - ATN/ status**

Bit 2 **MSG - MSG/ status**

Bit 1 **C/D - C/D status**

Bit 0 **I/O - I/O status**

When read, this register returns the SCSI control line status. A bit will be set when the corresponding SCSI control line is asserted. These bits are not latched; they are a true representation of what is on the SCSI bus at the time the register is read. This register can be used for diagnostics testing or operation in low level mode.

Writing to bits 7-2 has no effect.

Bits 1-0 **SSCF(1:0) - Synchronous SCSI Clock Frequency**

SSCF1	SSCF0	Synchronous CLK
0	0	Set by DCNTL
0	1	SCLK+1.0
1	0	SCLK+1.5
1	1	SCLK+2.0

When written, these bits determine the clock prescale factor used by the synchronous portion of the SCSI core. The default is to use the same clock prescale factor as the asynchronous logic (set by CF(1:0) in DCNTL). Setting one or both of these bits allows the synchronous logic to run at a different speed than the asynchronous logic; this is necessary for fast SCSI-2.

Register 0C Read Only
DMA Status (DSTAT)

7	6	5	4	3	2	1	0
DFE	RES	BF	ABRT	SSI	SIR	WTD	IID
1	0	0	0	0	0	0	0

Reading this register will clear any bits that are set at the time the register is read, but will not necessarily clear the register because additional interrupts may be pending (the 53C710 stacks interrupts). DMA interrupt conditions may be individually masked through the DIEN register.

If performing consecutive 8-bit reads of both the DSTAT and SSTAT0 registers (in either order), insert a delay equivalent to 12 BCLK periods between the reads to ensure the interrupts clear properly. Also, if reading both registers when both the ISTAT SIP and DIP bits may not be set, the SSTAT0 register should be read before the DSTAT register to avoid missing a SCSI interrupt. Both concerns are avoided if the registers are read together as a 32-bit longword.

Bit 7 **DFE - DMA FIFO Empty**

This status bit is set when the DMA FIFO is empty. This bit may be changing at the time this register is read. It may be used to determine if any data resides in the FIFO when an error occurs and an interrupt is generated. This bit is a pure status bit and will not cause an interrupt.

Bit 6 **RES - Reserved**

Bit 5 **BF - Bus Fault**

This bit is set when a host bus fault condition is detected. A host bus fault can only occur when the 53C710 is bus master, and is defined as a memory cycle that is ended by the assertion of BERR/ or TEA/.

Bit 4 **ABRT - Aborted**

This bit is set when an abort condition occurs. An abort condition occurs because of the

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following: the DP3_ABRT/ input signal is asserted by another device (parity generation mode) or a software abort command is issued by setting Bit 7 of the ISTAT register.

Bit 3 SSI - SCRIPT Step Interrupt

If the Single Step Mode bit in the DCNTL register is set, this bit will be set and an interrupt generated after successfully executing each SCRIPT instruction.

Bit 2 SIR - SCRIPT Interrupt Instruction Received

This status bit is set whenever an INTERRUPT instruction is evaluated as true.

Bit 1 WTD - Watchdog Timeout Detected

This status bit is set when the Watchdog Timer decrements to zero. The Watchdog Timer is only used for the Host memory interface. When the timer decrements to zero, it indicates that the memory system did not assert the acknowledge signal within the specified timeout period.

Bit 0 IID - Illegal Instruction Detected

This status bit will be set anytime an illegal instruction is decoded, whether the 53C710 is operating in single step mode or automatically executing SCSI SCRIPTs.

This bit will also be set if the 53C710 is executing a Wait Disconnect instruction and the SCSI REQ line is asserted without a disconnect occurring.

Register 0D SCSI Status Zero — Read Only (SSTAT0)

7	6	5	4	3	2	1	0
M/A	FCMP	STO	SEL	SGE	UDC	RST/	PAR
0	0	0	0	0	0	0	0

Reading this register will clear any bits that are set at the time the register is read, but will not necessarily clear the register because additional interrupts may be pending (the 53C710 stacks interrupts). SCSI interrupt conditions may be individually masked through the SIEN register.

If performing consecutive 8-bit reads of both the DSTAT and SSTAT0 registers (in either order), insert a delay equivalent to 12 BCLK periods between the reads to ensure the interrupts clear properly. Also, if reading both registers when both the ISTAT SIP and DIP bits may not be set, the SSTAT0 register should be read before the DSTAT register to avoid missing a SCSI interrupt. Both concerns are avoided if the registers are read together as a 32-bit longword.

Bit 7 M/A - Initiator Mode: Phase mismatch, or Target Mode: ATN/ active

In initiator mode, this bit is set if the SCSI phase asserted by the target does not match the SCSI phase defined in a Block Move instruction. The phase is sampled when REQ/ is asserted by the target. In target mode, this bit is set when the ATN/ signal is asserted by the initiator. This status bit is used in diagnostics testing or in low level mode.

Bit 6 FCMP - Function Complete

This bit is set when an arbitration only or full arbitration sequence has completed.

Bit 5 STO - SCSI Bus Timeout

This bit is set if one of the following conditions occurs:

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1) There is a selection or reselection timeout. A selection/reselection timeout occurs if the device being selected or reselected does not respond within the 250 msec timeout period.

2) The Wait for Disconnect takes longer than 250 msec. The Wait for Disconnect instruction has a bus activity timer that is reset by the physical disconnect.

3) No SCSI activity occurs for 250 msec while connected to the bus. There is a timer on all bytes (in all phases) sent or received on the SCSI bus. The timer is a bus activity timer that is reset by a byte going over the SCSI bus. If 250 milliseconds pass without a byte being moved, then a timeout will occur.

Bit 4 SEL - Selected or Reselected

This bit is set when the 53C710 is selected or reselected by another SCSI device. The Enable Selection and Reselection bit must have been set in the SCNTL1 register for the 53C710 to respond to selection and reselection attempts.

Bit 3 SGE - SCSI Gross Error

This bit is set when the 53C710 encounters a SCSI Gross Error condition. The following conditions can cause a SCSI Gross Error condition.

1) Data Underflow - the SCSI FIFO register was read when no data was present.

2) Data Overflow - Too many bytes were written to the SCSI FIFO or the synchronous offset caused the SCSI FIFO to be overwritten.

3) Offset Underflow - When the 53C710 is operating in target mode and an ACK/ pulse is received when the outstanding offset is zero.

4) Offset Overflow - the other SCSI device sent a REQ/ or ACK/ pulse with data which exceeded the maximum synchronous offset defined by the SXFER register.

5) Residual data in the Synchronous data FIFO - a transfer other than synchronous data receive was started with data left in the synchronous data FIFO.

6) A phase change occurred with an outstanding synchronous offset when the 53C710 is operating as an initiator.

Bit 2 UDC - Unexpected Disconnect

This bit is set when the 53C710 is operating in initiator mode and the target device unexpectedly disconnects from the SCSI bus. This bit is only valid when the 53C710 operates in the initiator mode. When the 53C710 is executing SCSI SCRIPTs, an unexpected disconnect is defined to be a disconnect that does not occur after receiving either a Disconnect Message (04h) or a Command Complete Message (00h). When the 53C710 operates in low level mode, any disconnect can cause an interrupt, even a valid SCSI disconnect.

This bit will also be set if a selection timeout occurs.

Bit 1 RST/ - SCSI RST/ Received

This bit is set when the 53C710 detects an active RST/ signal, whether the reset was generated external the chip or caused by the Assert RST/ bit in the SCNTL1 register. The 53C710 SCSI reset detection logic is edge-sensitive so that multiple interrupts will not be generated for a single assertion of the SCSI RST/ signal.

Bit 0 PAR - Parity Error

This bit is set when the 53C710 detects a parity error when sending or receiving SCSI data. The Enable Parity Checking bit (bit 3 in the SCNTL0 register) must be set for this bit to become active. A parity error can occur when receiving data from the SCSI bus or when receiving data from the host bus. From the host bus, parity is checked as it is transferred from the DMA FIFO to the SODL register. A parity error can occur from the host bus only if pass

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through parity is enabled (bit 3 in the SCNTL0 register = 1, bit 2 in the SCNTL0 register = 0).

Register 0E SCSI Status One — Read Only (SSTAT1)

7 ILF	6 ORF	5 OLF	4 AIP	3 LOA	2 WOA	1 RST/	0 SDP/
0	0	0	0	0	0	0	0

Bit 7 ILF - SIDL Register Full

This bit is set when the SCSI Input Data Latch register (SIDL) contains data. Data is transferred from the SCSI bus to the SCSI Input Data Latch register before being sent to the DMA FIFO and then to the host bus. The SIDL register contains SCSI data received asynchronously. Synchronous data received does not flow through this register.

Bit 6 ORF - SODR Register Full

This bit is set when the SCSI Output Data Register (SODR, a hidden buffer register which is not accessible) contains data. The SODR register is used by the SCSI logic as a second storage register when sending data synchronously. It is a not accessible to the user (cannot be read or written). This bit can be used to determine how many bytes reside in the chip when an error occurs.

Bit 5 OLF - SODL Register Full

This bit is set when the SCSI Output Data Latch (SODL) contains data. The SODL register is the interface between the DMA logic and the SCSI bus. In synchronous mode, data is transferred from the host bus to the SCSI Output Data Register (SODR, a hidden buffer register which is not accessible), and then to the SODL register before being sent to the SCSI bus. In asynchronous mode, data is transferred from the host bus to the SODL register, and then to the SCSI bus. The SODR buffer register is not used for asynchronous transfers. This bit can be used to determine how many bytes reside in the chip when an error occurs.

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Bit 4 AIP - Arbitration In Progress

Arbitration in Progress (AIP = 1) indicates that the 53C710 has detected a bus free condition, asserted BSY and asserted its SCSI ID onto the SCSI bus.

Bit 3 LOA - Lost Arbitration

When set, LOA indicates that the 53C710 has detected a bus free condition, arbitrated for the SCSI bus, and lost arbitration due to another SCSI device asserting the SEL/ signal.

Bit 2 WOA - Won Arbitration

When set, WOA indicates that the 53C710 has detected a bus free condition, arbitrated for the SCSI bus and won arbitration. The arbitration mode selected in the SCNTL0 register must be Full Arbitration & Selection for this bit to be set.

Bit 1 RST/ - SCSI RST/ Signal

This bit represents the current status of the SCSI RST/ signal. This signal is not latched and may be changing when read.

Bit 0 SDP/ - SCSI SDP/ Parity Signal

This bit represents the current status of the SCSI SDP/ parity signal. This signal is not latched and may be changing when read.

Register 0F SCSI Status Two — Read Only (SSTAT2)

7	6	5	4	3	2	1	0
FF3	FF2	FF1	FF0	SDP	MSG	C/D	I/O
0	0	0	0	0	0	0	0

Bits 7-4 FF(3:0) - FIFO Flags

FF3	FF2	FF1	FF0	Bytes in SCSI FIFO
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8

These four bits define the number of bytes that currently reside in the 53C710's SCSI synchronous data FIFO. These bits are not latched and they will change as data moves through the FIFO. Because the FIFO is only 8 bytes deep, values over 8 will not occur.

Bit 3 SDP - Latched SCSI Parity

This bit reflects the SCSI parity signal (SDP/) corresponding to the data latched in the SCSI Input Data Latch register (SIDL). It changes when a new byte is latched into the SIDL register. This bit is active high, ie. it is set when the parity signal is active.

Bit 2 MSG - SCSI MSG/ signal

Bit 1 C/D - SCSI C/D signal

Bit 0 I/O - SCSI I/O signal

These SCSI phase status bits are latched on the asserting edge of REQ/ when operating in either initiator or target mode. These bits are set when the corresponding signal is active. They are useful when operating in Low Level mode.

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Registers 10-13 Read/Write
Data Structure Address (DSA)

This register contains the base address used for all table indirect calculations. It is 32-bits wide and defaults to all zeros.

During any Memory-to-Memory Move operation, the contents of this register are destroyed. If the DSA value is needed for a subsequent SCSI SCRIPT, save and later restore it.

Register 14 Read Only
Chip Test Zero (CTEST0)

7	6	5	4	3	2	1	0
RES	RES	RES	RES	RES	RES	RES	DDIR
X	X	X	X	X	X	X	0

X = Don't Care/Indeterminate

Bits 7-1 RES - Reserved

Bit 0 DDIR - Data Transfer Direction

This status bit indicates which direction data is being transferred. When this bit is set, the data will be transferred from the SCSI bus to the host bus. When this bit is clear, the data will be transferred from the host bus to the SCSI bus.

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Register 15 Chip Test One — Read Only (CTEST1)

7	6	5	4	3	2	1	0
FMT3	FMT2	FMT1	FMT0	FFL3	FFL2	FFL1	FFL0
1	1	1	1	0	0	0	0

Bits 7-4 FMT(3:0) - Byte Empty in DMA FIFO

These bits identify the bottom bytes in the DMA FIFO that are empty. Each bit corresponds to a byte lane in the DMA FIFO. For example, if byte lane 3 is empty, then FMT3 will be 1. Since the FMT flags indicate the status of bytes at the bottom of the FIFO, if all FMT bits are set, the DMA FIFO is empty.

Bits 3-0 FFL(3:0) - Byte Full in DMA FIFO

These status bits identify the top bytes in the DMA FIFO that are full. Each bit corresponds to a byte lane in the DMA FIFO. For example, if byte lane 3 is full, then FFL3 will be 1. Since the FFL flags indicate the status of bytes at the top of the FIFO, if all FFL bits are set, the DMA FIFO is full.

Register 16 Chip Test Two — Read Only (CTEST2)

7	6	5	4	3	2	1	0
RES	SIGP	SOFF	SFP	DFP	TEOP	DREQ	DACK
0	0	1	0	0	0	0	1

Bit 7 RES - Reserved

Bit 6 SIGP - Signal Process

This bit is a copy of the SIGP bit in the ISTAT register (bit 5). The SIGP bit is used to signal a running SCRIPT. When this bit is read, the SIGP bit in the ISTAT register is cleared.

Bit 5 SOFF - SCSI Offset Compare

Whether the chip is an initiator or target determines how this bit will operate. If the 53C710 is an initiator, this bit will be 1 whenever the SCSI Synchronous offset counter is equal to zero. If the 53C710 is a target, this bit will be 1 whenever the SCSI Synchronous offset counter is equal to the maximum synchronous offset defined in the SXFER register.

Bit 4 SFP - SCSI FIFO parity

This bit represents the parity bit of the SCSI Synchronous FIFO corresponding to data read out of the FIFO. Reading the CTEST3 register unloads a data byte from the bottom of the SCSI synchronous FIFO. When the CTEST3 register is read, the data parity bit is latched into this bit location.

Bit 3 DFP - DMA FIFO Parity

This bit represents the parity bit of the DMA FIFO when the CTEST6 register reads data out of the FIFO. Reading the CTEST6 register unloads one data byte from the bottom of the DMA FIFO. When the CTEST6 register is read the parity signal is latched into this bit location and the next byte falls down to the bottom of the FIFO.

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Bit 2 **TEOP - SCSI True End of Process**

This bit indicates the status of the 53C710's internal TEOP signal. The TEOP signal acknowledges the completion of a transfer through the SCSI portion of the 53C710. When this bit is set, TEOP is active. When this bit is clear, TEOP is inactive.

Bit 1 **DREQ - Data Request Status**

This bit indicates the status of the 53C710's internal Data Request signal (DREQ). When this bit is set, DREQ is active. When this bit is clear, DREQ is inactive.

Bit 0 **DACK - Data Acknowledge Status**

This bit indicates the status of the 53C710's internal Data Acknowledge signal (DACK/). When this bit is set, DACK/ is inactive. When this bit is clear, DACK/ is active.

Register 17 Chip Test Three — Read Only (CTEST3)

7	6	5	4	3	2	1	0
SF7	SF6	SF5	SF4	SF3	SF2	SF1	SF0
0	0	0	0	0	0	0	0

Bits 7-0 **SF(7:0) - SCSI FIFO**

Reading this register unloads the bottom byte of the eight byte SCSI Synchronous FIFO. Reading this register also latches the parity bit for the FIFO into the SCSI FIFO Parity bit in the CTEST2 register. The FIFO Full Bits in the SSTAT2 register can be read to determine how many bytes currently reside in the SCSI Synchronous FIFO. Reading this register when the SCSI FIFO is empty causes a SCSI Gross Error (FIFO underflow).

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Register 18 Chip Test Four — Read/Write (CTEST4)

7	6	5	4	3	2	1	0
MUX	ZMOD	SZM	SLBE	SFWR	FBL2	FBL1	FBL0
0	0	0	0	0	0	0	0

Bit 7 MUX - Host Bus Multiplex Mode

When set, the MUX bit puts the 53C710 into Host Bus MUX Mode. In this mode, the chip asserts a valid address for one BCLK (during which AS/TS is valid and the data bus is three-stated), and then three-states the address bus and drives the data bus (if a write). This allows the address and data buses to be tied together. It should be written prior to acquiring bus mastership.

Bit 6 ZMOD - High Impedance Mode

Setting this bit causes the 53C710 to place all output and bidirectional pins into a high-impedance state. In order to read data out of the 53C710, this bit must be cleared.

This bit is intended for board-level testing only. Setting this bit during system operation will likely result in a crash.

Bit 5 SZM - SCSI High-Impedance Mode

Setting this bit causes the 53C710 to place certain SCSI outputs in a high-impedance state. The following outputs will be in a high-impedance state: SD(7:0), SDP, BSY/, SEL/, RST/, REQ/, C/D, I/O, MSG/, ACK/, ATN/. The direction control lines (SDIR(7:0), SDIRP, BSYDIR, RSTDIR, and SELDIR) are deasserted low and will not be in a high-impedance state. In order to transfer data on the SCSI bus, this bit must be cleared.

Bit 4 SLBE - SCSI Loopback Enable

Setting this bit enables "Loopback" mode. Loopback allows any SCSI signal to be asserted. 53C710 may be an initiator or a target. It also allows the 53C710 to transfer data from the SODL register back into the

SIDL register. For a complete description of the tests that can be performed in loopback mode, please refer to the "Loopback Mode" section.

Bit 3 SFWR - SCSI FIFO Write Enable

Setting this bit redirects data from the SODL to the SCSI FIFO. A write to the SODL register loads a byte into the SCSI FIFO. The parity bit loaded into the FIFO will be odd or even parity depending on the status of the Assert SCSI Even Parity bit in the SCNTL1 register. Clearing this bit will disable this feature.

Bits 2-0 FBL(2:0) - FIFO Byte Control

FBL2	FBL1	FBL0	DMA FIFO Byte Lane	Pins
0	X	X	disabled	n/a
1	0	0	0	D(7:0)
1	0	1	1	D(15:8)
1	1	0	2	D(23:16)
1	1	1	3	D(31:24)

These bits send the contents of the CTEST6 register to the appropriate byte lane of the 32-bit DMA FIFO. If the FBL2 bit is set, then FBL1 & FBL0 determine which of four byte lanes can be read or written. Each of the four bytes that make up the 32-bit DMA FIFO can be accessed by writing these bits to the proper value. For normal operation, FBL2 must equal zero (set to this value before executing SCSI SCRIPTs).

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Register 19 Chip Test Five — Read/Write (CTEST5)

7	6	5	4	3	2	1	0
ADCK	BBCK	ROFF	MASR	DDIR	EOP	DREQ	DACK
0	0	0	0	0	0	0	0

Bit 7 ADCK - Clock Address Incrementer

Setting this bit increments the address pointer contained in the DNAD register (by four bytes). The DNAD register is incremented based on the DNAD contents and the current DBC value. This bit automatically clears itself after incrementing the DNAD register.

Bit 6 BBCK - Clock Byte Counter

Setting this bit decrements the byte count contained in the DBC register. The DBC register supports only 24-bits. It is decremented based on the DBC contents and the current DNAD value. This bit automatically clears itself after decrementing the DBC register.

Bit 5 ROFF - Reset SCSI Offset

Setting this bit clears the current offset pointer in the SCSI synchronous offset counter. This bit is set if a SCSI Gross Error condition occurs. The offset should be cleared when a synchronous transfer does not complete successfully. This bit automatically clears itself after clearing the synchronous offset.

Bit 4 MASR - Master Control for Set or Reset pulses

This bit controls the operation of bits 3-0. When this bit is set, bits 3-0 assert the corresponding signals. When this bit is reset, bits 3-0 deassert the corresponding signals. This bit and bits 3-0 should not be changed in the same write cycle.

Bit 3 DDIR - DMA Direction

Setting this bit either asserts or deasserts the internal DMAWR direction signal depending on the current status of the MASR bit in this register. Asserting the DMAWR signal indicates that data will be transferred from the SCSI bus to the host bus. Deasserting the DMAWR signal transfers data from the host bus to the SCSI bus.

Bit 2 EOP - End of Process

Setting this bit either asserts or deasserts the internal EOP control signal depending on the current status of the MASR bit in this register. The internal EOP signal is an output from the DMA portion of the 53C710 to the SCSI portion of the 53C710. Asserting the EOP signal indicates that the last data byte has been transferred between the two portions of the chip. Deasserting the EOP signal indicates that the last data byte has not been transferred between the two portions of the chip. If the MASR bit is configured to assert this signal, this bit automatically clears itself after pulsing the EOP signal.

Bit 1 DREQ - Data Request

Setting this bit either asserts or deasserts the internal DREQ (data request signal) depending on the current status of the MASR bit in this register. Asserting the DREQ signal indicates that the SCSI portion of the 53C710 requests a data transfer with the DMA portion of the chip. Deasserting the DREQ signal indicates that data should not be transferred between the SCSI portion of the 53C710 and the DMA portion. If the MASR bit is configured to assert this signal, this bit automatically clears itself after asserting the DREQ signal.

Bit 0 DACK - Data Acknowledge

Setting this bit either asserts or deasserts the internal DACK/ data request signal dependent on the current status of the MASR bit in this register. Asserting the DACK/ signal indicates that the DMA portion of the 53C710 acknowledges a data transfer with the SCSI

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portion of the chip. Deasserting the DACK/ signal indicates that data should not be transferred between the DMA portion of the 53C710 and the SCSI portion. If the MASR bit is configured to assert this signal, this bit automatically clears itself after asserting the DACK/ signal.

Register 1A Chip Test Six — Read/Write (CTEST6)

7	6	5	4	3	2	1	0
DF7	DF6	DF5	DF4	DF3	DF2	DF1	DF0
0	0	0	0	0	0	0	0

Bits 7-0 DF(7:0) - DMA FIFO

Writing to this register writes data to the appropriate byte lane of the DMA FIFO as determined by the FBL bits in the CTEST4 register. Reading this register unloads data from the appropriate byte lane of the DMA FIFO as determined by the FBL bits in the CTEST4 register. Data written to the FIFO is loaded into the top of the FIFO. Data read out of the FIFO is taken from the bottom. When data is read from the DMA FIFO, the parity bit for that byte is latched and stored in the DMA FIFO parity bit in the CTEST2 register.

To prevent DMA data from being corrupted, this register should not be accessed before starting or restarting a SCRIPT.

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Register 1B Chip Test Seven — Read /Write (CTEST7)

7	6	5	4	3	2	1	0
CDIS	SC1	SC0	Notime	DFP	EVP	TT1	DIFF
0	0	0	0	0	0	0	0

Bit 7 CDIS - Cache Burst Disable

When this bit is set, the 53C710 will not request a Cache-Line Burst. When this bit is clear, the chip will attempt Cache-Line bursts when all necessary conditions are met.

Bits 6-5 SC(1:0) - Snoop Control

The values of these bits are asserted on the corresponding device pins during bus mastership if bit 0 of CTEST8 is clear. Otherwise, the SC1 pin will always be driven with the value of the SC1 bit, and the SC0 pin will reflect the state of the internal Host Cycle Request signal.

Bit 4 Notime - Selection Timeout Disable

Setting this bit disables the 250 ms timer for all modes, including byte to byte.

Bit 3 DFP - DMA FIFO Parity

This bit represents the parity bit of the DMA FIFO when reading data out of the DMA FIFO via programmed I/O. In order to transfer data to/from the DMA FIFO, perform a read or a write to the CTEST6 register. When loading data into the FIFO via programmed I/O, write this bit to the FIFO as the parity bit for each byte loaded. When writing data to the DMA FIFO, set this bit with the status of the parity bit to be written to the FIFO before writing the byte to the FIFO. For the details of performing a diagnostic test of the DMA FIFO, please refer to the section on "Diagnostics".

Bit 2 EVP - Even Parity

Parity is generated for all slave mode register reads and master mode memory writes. This bit controls the parity sense.

Setting this bit causes the 53C710 to generate even parity when driving data on the host data bus. The 53C710 inverts the parity bit received from the SCSI bus to create even parity. In addition, the even parity received from the host bus is inverted to odd parity before the 53C710 checks parity and sends the data to the SCSI bus. Clearing this bit causes the 53C710 to maintain odd parity throughout the chip.

Bit 1 TT1 - Transfer Type Bit

The value of this bit is asserted on the TT1 pin during bus mastership (synchronous host bus mode only). This bit is not used in asynchronous host bus mode.

Bit 0 DIFF - Differential Mode

Setting this bit enables the 53C710 to interface with external differential pair transceivers. The function of the SCSI BSY/, SEL/, and RST/, is different for differential mode. For more information on differences between the two modes, refer to the pin descriptions for these signals. Resetting this bit enables single-ended mode. This bit should be set in the initialization routine if the differential pair interface is to be used.

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Registers 1C-1F Temporary Stack — Read/Write (TEMP)

This 32-bit register stores the instruction address pointer for a CALL or a RETURN instruction. The address pointer stored in this register is loaded into the DSP register. This address points to the next instruction to be executed. Do not write to TEMP while the 53C710 is executing SCSI SCRIPTs.

During any Memory-to-Memory Move operation, the contents of this register are destroyed. If the DSA value is needed for a subsequent SCSI SCRIPT, save and then later restore it.

Register 20 DMA FIFO — Read/Write (DFIFO)

7	6	5	4	3	2	1	0
RES	BO6	BO5	BO4	BO3	BO2	BO1	BO0
0	0	0	0	0	0	0	0

Bit 7 RES - Reserved

Bits 6-0 BO(6:0) - Byte Offset Counter

These six bits indicate the amount of data transferred between the SCSI core and the DMA core. It may be used to determine the number of bytes in the DMA FIFO when a DMA error occurs. These bits are unstable while data is being transferred between the two cores; once the chip has stopped transferring data, these bits are stable.

The following steps will determine how many bytes are left in the DMA FIFO when an error occurs, regardless of the direction of the transfer:

1) Subtract the 7 least-significant bits of the DBC register from the 7-bit value of the DFIFO register

2) AND the result with 7Fh for a byte count between zero and 64

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Register 21 Interrupt Status (ISTAT) — Read/Write

7 ABRT	6 RST	5 SIGP	4 RES	3 CON	2 RES	1 SIP	0 DIP
0	0	0	0	0	0	0	0

This is the only register that can be accessed by the host CPU while the 53C710 is executing SCRIPTs (without interfering in the operation of the 53C710). It may be used to poll for interrupts if interrupts are disabled. There may be stacked interrupts pending; read this register after clearing an interrupt to check for stacked interrupts.

Bit 7 ABRT - Abort Operation

Setting this bit aborts the current operation being executed by the 53C710. If this bit is set and an interrupt is received, reset this bit before reading the DSTAT register to prevent further Aborted interrupts from being generated. The sequence to abort any operation is:

1) Set this bit
2) Wait for an interrupt
3) Read the ISTAT register
4) If the SCSI Interrupt Pending bit is set, then read the SSTAT0 register to determine the cause of the SCSI Interrupt and go back to step 2
5) If the SCSI Interrupt Pending bit is clear, and the DMA Interrupt Pending bit is set, then write 00h value to this register
6) Read the DSTAT register to verify the aborted interrupt and to see if any other interrupting conditions have occurred.

Bit 6 RST - Software Reset

Setting this bit resets the 53C710. All registers are cleared to their respective default values and all SCSI signals are deasserted. Setting this bit does not cause the SCSI RST/ signal to be asserted. This bit is not self-clearing; it must be cleared to clear the reset condition (a hardware reset will also clear this bit).

Bit 5 SIGP - Signal Process

SIGP (SIGnal Process) is a R/W bit that can be written at any time, and polled & reset via CTEST2. The SIGP bit can be used in various ways to pass a flag to or from a running SCRIPT.

The only SCRIPT instruction directly affected by the SIGP bit is Wait For Selection/Reselection. Setting this bit causes that opcode to jump to the alternate address immediately. The instructions at the alternate jump address should check the status of SIGP to determine the cause of the jump. The SIGP bit may be used at any time and is not restricted to the wait for selection/ reselection condition.

Note: If the SIGP bit is active when a selection/reselection occurs, the auto-switching from/to target mode will be disabled and must be manually set by either the host or a SCRIPT.

Bit 4 RES - Reserved

Bit 3 CON - Connected

This bit is automatically set anytime the 53C710 is connected to the SCSI bus as an initiator or as a target. It will be set after successfully completing arbitration or when the 53C710 has responded to a bus-initiated selection or reselection. It will also be set after successfully completing arbitration when operating in low level mode. When this bit is clear, the 53C710 is not connected to the SCSI bus.

Bit 2 RES - Reserved

Bit 1 SIP - SCSI Interrupt Pending

This status bit is set when an interrupt condition is detected in the SCSI portion of the 53C710. The following conditions will cause a SCSI interrupt to occur:

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- A phase mismatch (initiator mode) or ATN/ becomes active (target mode)
- An arbitration sequence complete
- A selection or reselection timeout occurs
- The 53C710 was selected or reselected
- A SCSI gross error occurs
- An unexpected disconnect occurs
- A SCSI reset occurs
- A parity error is detected

To determine exactly which condition(s) caused the interrupt, the SSTAT0 register should be read.

Bit 0 DIP - DMA Interrupt Pending

This status bit is set when an interrupt condition is detected in the DMA portion of the 53C710. The following conditions will cause a DMA interrupt to occur:

- The DMA FIFO is empty
- A bus fault is detected
- An abort condition is detected
- A SCRIPT instruction is executed in single step mode
- A SCRIPT interrupt instruction is executed
- The Watchdog Timer decrements to zero.
- An illegal instruction is detected

To determine exactly which condition(s) caused the interrupt, the DSTAT register should be read.

Register 22 Chip Test Eight — Read/Write (CTEST8)

7	6	5	4	3	2	1	0
V3	V2	V1	V0	FLF	CLF	FM	SM
V	V	V	V	0	0	0	0

Bits 7-4 V(3:0) - Chip Revision Level

These bits identify the chip revision level for software purposes. This data sheet applies to devices with revision level 0.

Bit 3 FLF - Flush DMA FIFO

When this bit is set, data residing in the DMA FIFO is transferred to/from memory, starting at the address in the DNAD register. The internal DMAWR signal, controlled by the CTEST5 register, determines the direction of the transfer. This bit is not self clearing; once the 53C710 has successfully transferred the data, this bit should be reset.

Bit 2 CLF - Clear DMA and SCSI FIFOs

When this bit is set, all data pointers for the SCSI and DMA FIFOs are cleared. In addition to the SCSI and DMA FIFO pointers, the SIDL, SODL, and SODR full bits in the SSTAT1 register are cleared. Any data in either of the FIFOs is lost. This bit automatically resets after the 53C710 has successfully cleared the appropriate FIFO pointers and registers.

Bit 1 FM - Fetch Pin Mode

When set, this bit causes the FETCH/ pin to deassert during indirect and table indirect read operations. FETCH/ will only be active during the opcode portion of an instruction fetch. This allows SCRIPTs to be stored in a PROM while data tables are stored in RAM.

If this bit is not set, FETCH/ will be asserted for all bus cycles during instruction fetches.

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Bit 0 SM - Snoop Pins Mode

When set, the two snoop pins change functions and become pure outputs that are always driven, except when in ZMODE.

Pin	Function
SC0	Becomes a copy of the internal bus request signal. Signal will assert prior to BR/ and will be negated during the AS/ of the last bus cycle.
SC1	Drives the value in the SC1 register bit.

When clear, the snoop pins are driven during host bus ownership with the values of the CTEST7 SC(1:0) bits.

Register 23 Longitudinal Parity (LCRC) Read/Write

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0

Bits 7-0 Longitudinal Parity

This register contains the longitudinal parity for all data crossing from the DMA FIFO to/from the SCSI core. The parity will consist of an exclusive OR of all data bytes.

Any write to this register will clear its contents to 00H regardless of the value written.

Like the SFBR, this register is used by the SCSI core to hold the SCSI ID value during selection and reselection. The LCRC register should be used instead of the SFBR because the SFBR is used as an accumulator during many SCRIPT operations, and may be overwritten at any time by a selection or reselection.

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Registers 24-26 DMA Byte Counter — Read/Write (DBC)

Default: all zeros

This 24-bit register determines the number of bytes to be transferred in a Block Move instruction. While sending data to the SCSI bus, the counter is decremented as data is moved into the DMA FIFO from memory. While receiving data from the SCSI bus, the counter is decremented as data is written to memory from the 53C710. The DBC counter is decremented each time that the AS/ signal is pulsed by the 53C710. It is decremented by an amount equal to the number of bytes that were transferred.

The maximum number of bytes that can be transferred in any one Block Move command is 16,777,215 bytes. The maximum value that can be loaded into the DBC register is FFFFFFh. If the instruction is Block Move and a value of 000000h is loaded into the DBC register, an illegal instruction interrupt will occur if not a target mode Command Phase.

The DBC Register is also used during table indirect I/O SCRIPTs to hold the offset value.

Register 27 DMA Command — Read/Write (DCMD)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0

Bits 7-0 DMA Command

This 8-bit register determines the instruction for the 53C710 to execute. This register has a different function for each instruction. For a complete description, refer to the 53C710 instruction set.

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Registers 28-2B Read/Write
DMA Next Data Address (DNAD)

Default: all zeros

This 32-bit register contains the general purpose address pointer. At the start of some SCRIPT operations, its value is copied from the DSPS register. Its value may not be valid except in certain abort conditions.

To maintain software compatibility with the 53C700, interrupt vectors should be read from the DSPS register.

Registers 2C-2F Read/Write
DMA SCRIPTs Pointer (DSP)

Default: all zeros

To execute SCSI SCRIPTs, the address of the first SCSI SCRIPT must be written to this register. In normal SCRIPT operation, once the starting address of the SCSI SCRIPTs is written to this register, the SCRIPTs are automatically fetched and executed until an interrupt condition occurs.

In single step mode, there is a SCRIPT step interrupt after each instruction is executed. The DSP register does not need to be written with the next address, but the Start DMA bit (bit 2, DCNTL register) must be set each time the step interrupt occurs to fetch and execute the next SCSI SCRIPT. When writing this register 8 bits at a time, writing the upper 8 bits begins execution of the SCSI SCRIPTs.

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Register 30-33 Read/Write
DMA Scripts Pointer Save (DSPS)

Default: all zeros

This register contains the second longword of Read/Write or Transfer Control SCRIPT instruction. It is overwritten each time a SCRIPT instruction is executed. When a SCRIPT interrupt is fetched, this register holds the interrupt vector.

Registers 34-37 Read/Write
Scratch Register (SCRATCH)

Default: all zeros

This is a general purpose user definable scratch pad register. Normal SCRIPT operations will not destroy the contents of this register; only Register Read/Write and Memory Moves into the SCRATCH register will alter its contents.

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Register 38 DMA Mode (DMODE) — Read/Write

7	6	5	4	3	2	1	0
BL1	BL0	FC2	FC1	PD	FAM	U0	MAN
0	0	0	0	0	0	0	0

Bit 7-6 BL(1:0) - Burst Length

BL1	BL0	Burst Length
0	0	1 Transfer Burst
0	1	2 Transfer Burst
1	0	4 Transfer Burst
1	1	8 Transfer Burst

These bits control the number of bus cycles performed per bus ownership. The 53C710 asserts the Bus Request output when the DMA FIFO can accommodate a transfer of at least one burst size of data. Bus Request is also asserted during start-of-transfer/end-of-transfer cleanup & alignment, even though less than a full burst of transfers may be performed.

To perform Cache-Line bursts, these bits must be set to 4 or 8 transfers and cache bursting must be enabled (CTEST7).

The 53C710 inserts a "fairness delay" of approximately 5 to 8 BCLKs between bus ownerships. This gives the CPU and other bus master devices the opportunity to access memory between bursts.

Bit 5-4 FC(2:1) - Function Code

These bits are user defined. Their values are asserted onto the corresponding device pins during bus mastership. These bits/pins are active in both bus modes.

Bit 3 PD - Program/Data

This bit affects the function of the FC0/ pin. Setting this bit causes the 53C710 to drive the FC0/ signal low when fetching instructions from memory. Clearing this bit causes the 53C710 to drive the FC0/ signal high when fetching instructions from memory.

The FC0/ signal is always driven high when moving data to/from memory and can only be driven low during instruction fetch cycles. This feature can be used to allow SCRIPTs and data to be stored in separate memory banks.

Bit 2 FAM - Fixed Address Mode

Setting this bit disables the address pointer (DNAD register) so that it will not increment after each data transfer. If this bit is clear, the pointer increments after each data transfer. This bit is used to transfer data to/from a fixed port address. The port width must be 32 bits.

Bit 1 U0/TT0 - User Programmable Transfer Type

In both bus modes, UPSO-TT0/ is a general purpose output pin. The value in the register bit is asserted onto the UPSO-TT0/ pin while the 53C710 is a bus master.

Bit 0 MAN - Manual Start Mode

Clearing this bit causes the 53C710 to automatically fetch and execute SCSI SCRIPTs after the DSP register is written. Setting this bit disables the 53C710 from automatically fetching and executing SCSI SCRIPTs after the DSP register is written. When the Start DMA bit in the DCNTL register is cleared, it controls the start time of the operation. Once the Start DMA bit in the DCNTL register is set, the 53C710 automatically fetches and executes each instruction.

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Register 39 DMA Interrupt Enable (DIEN) — Read/Write

7	6	5	4	3	2	1	0
RES	RES	BF	ABRT	SSI	SIR	WTD	IID
0	0	0	0	0	0	0	0

Bits 7-6 **RES - Reserved**

Bit 5 **BF - Bus Fault**

Bit 4 **ABRT - Aborted**

Bit 3 **SSI - SCRIPT Step Interrupt**

Bit 2 **SIR - SCRIPT Interrupt Instruction Received**

Bit 1 **WTD - Watchdog Timeout Detected**

Bit 0 **IID - Illegal Instruction Detected**

This register contains the interrupt mask bits corresponding to the interrupting conditions described in the SSTAT0 register. Clearing a mask bit prevents IRQ/ from being asserted and ISTAT DIP from being set for the corresponding interrupt, but the status bit will still be set in the SSTAT0 register. Setting a mask bit enables the assertion of IRQ/ for the corresponding interrupt.

Register 3A DMA Watchdog Timer (DWT) — Read/Write

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0

Bits 7-6 **DMA Watchdog Timer**

The DMA Watchdog Timer Register provides a timeout mechanism during data transfers between the 53C710 and memory. This register determines the amount of time that the 53C710 will wait for the assertion of the Transfer Acknowledge/ signal after starting a bus cycle. Write the timeout value to this register during initialization. Every time that the 53C710 transfers data to/from memory, the value stored in this register is loaded into the counter. Disable the timeout feature by writing 00h to this register.

The unit time base for this register is 16*BCLK input period. For example, at 50 MHz the time base for this register is 16 x 20 ns = 320 ns. If a timeout of 50 µsec is desired, then this register should be loaded with a value of 9Dh.

The minimum timeout value that should be loaded into this register is 02h; the value 01h will not provide a reliable timeout period.

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Register 3B DMA Control Register — Read/Write (DCNTL)

7	6	5	4	3	2	1	0
CF1	CF0	EA	SSM	LLM	STD	FA	COM
0	0	0	0	0	0	0	0

Bit 7-6 CF(1:0) - Clock Frequency

CF1	CF0	SCSI Core Clock	SCLK Frequency
1	1	SCLK+3	50.01 - 66.00 MHz
0	0	SCLK+2	37.51 - 50.00 MHz
0	1	SCLK+1.5	25.01 - 37.50 MHz
1	0	SCLK+1	16.67 - 25.00 MHz

These two bits determine the SCLK prescale factor used by the 53C710 SCSI core; the internal SCSI clock is derived from the externally applied SCLK. The above table describes how to program these two bits.

Note: It is important that these bits be set to the proper values to guarantee that the 53C710 meets the SCSI timings as defined by the ANSI specification. These bits affect both asynchronous and synchronous timings (unless the synchronous clock is decoupled via the SBCL register).

Bit 5 EA - Enable Ack

Setting this bit will cause the STERM/-TA pin to become bidirectional, ie. the 53C710 will generate STERM/-TA during slave accesses. When this bit is clear, the 53C710 will monitor STERM/-TA to determine the end of a cycle. This bit takes effect during the cycle in which it is set; setting this bit must be the first I/O performed to the 53C710 if this feature is desired.

Bit 4 SSM - Single Step Mode

Setting this bit causes the 53C710 to stop after executing each SCRIPT instruction, and generate a SCRIPT Step interrupt. When this bit is clear the 53C710 will not stop after each instruction; instead it continues fetching and executing instructions until an interrupt condition occurs. For normal SCSI SCRIPTs operation, this bit should be clear. To restart the 53C710 after it generates a SCRIPT Step interrupt, the ISTAT and DSTAT registers should be read to clear the interrupt and then the START DMA bit in this register should be set.

Bit 3 LLM - Enable SCSI Low Level Mode

Setting this bit places the 53C710 in low level mode. In this mode, no DMA operations can occur, and no SCRIPT instructions can be executed. Arbitration and selection may be performed by setting the Start Sequence bit as described in the SCNTL0 register. SCSI bus transfers are performed by manually asserting and polling SCSI signals. Clearing this bit allows instructions to be executed in SCSI SCRIPTs mode.

Bit 2 STD - Start DMA Operation

The 53C710 fetches a SCSI SCRIPT instruction from the address contained in the DSP register when this bit is set. This bit is required if the 53C710 is in one of the following modes:

1) Manual Start Mode - Bit 0 in the DMODE register is set

2) Single Step Mode - Bit 4 in the DCNTL register is set

When the 53C710 is executing SCRIPTs in manual start mode, the Start DMA bit needs to be set to start instruction fetches, but does not need to be set again until an interrupt occurs. When the 53C710 is in single step mode, the Start DMA bit needs to be set to restart execution of SCRIPTs after a single step interrupt.

Bit 1 FA - Fast Arbitration

When this bit is set, the 53C710 will immediately become bus master after receiving a bus grant, saving one clock cycle of arbitration time. When this bit is clear, the

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53C710 will follow the normal arbitration sequence.

Bit 0 COM - 53C700 Compatibility

When this bit is clear, the 53C710 will behave in a manner compatible with the 53C700; selection/reselection IDs will be stored in both the LCRC and SFBR registers, and auto switching is enabled.

When this bit is set, the ID will be stored only in the LCRC register, protecting the SFBR from being overwritten should a selection/ reselection occur during a DMA register to register operations. The default condition of this bit (clear) causes the 53C710 to act the same as the 53C700, which does not support register to register operations. Also, when this bit is set auto switching is disabled.

Register 3C-3F Adder Sum Output — Read (ADDER)

This register contains the output of the internal adder, and is used primarily for test purposes.

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SCSI SCRIPTs

After power up and initialization of the 53C710, the chip may be operated in one of two modes:

1) Low level register interface

2) SCSI SCRIPTs mode

In the low level register interface, the user has access to the DMA control logic and the SCSI bus control logic. The chip may be operated much like an NCR 53C80. An external processor has access to the SCSI bus signals and the low level DMA signals which allows a complicated board level test algorithm to be devised. The interface is useful for backward compatibility with SCSI devices that require certain unique timings or bus sequences to operate properly, Another feature allowed at the low level is loopback testing. In Loopback Mode, the SCSI core can be directed to talk to the DMA core to test internal data paths all the way out to the chip's pins.

Operating in the SCSI SCRIPTs mode, the 53C710 requires only a SCRIPTs start address. All commands are fetched from external memory. The 53C710 fetches and executes its own instructions by becoming a bus master on the host bus and fetching two or three 32-bit words into its registers. Commands are fetched until an interrupt command is encountered, or until an unexpected event (e.g. hardware error detected) causes an interrupt to the external processor.

Once an interrupt is generated, the 53C710 halts all operations until the interrupt is serviced. Then, the start address of the next SCRIPT instruction may be written to the DSP register to restart the automatic fetch and execution of instructions.

The SCSI SCRIPTs mode of execution allows the 53C710 to make decisions based on the status of the SCSI bus, thereby off-loading the microprocessor from servicing numerous interrupts.

Given the rich set of SCSI oriented features included in the command set, and the ability to re-enter the SCSI algorithm at any point, this high level interface is all that is required for both normal and exception conditions. Therefore, switching to low level mode for error recovery should never be required.

There are five types of instructions implemented in the 53C710: Block Move; I/O; Transfer Control; Memory Move; and Read/Write. Each instruction consists of two or three 32-bit words. The first 32-bit word is always loaded into the DCMD and DBC registers, the second into the DSPS register. The third word, only used by Memory Move instructions, is loaded into the TEMP register.

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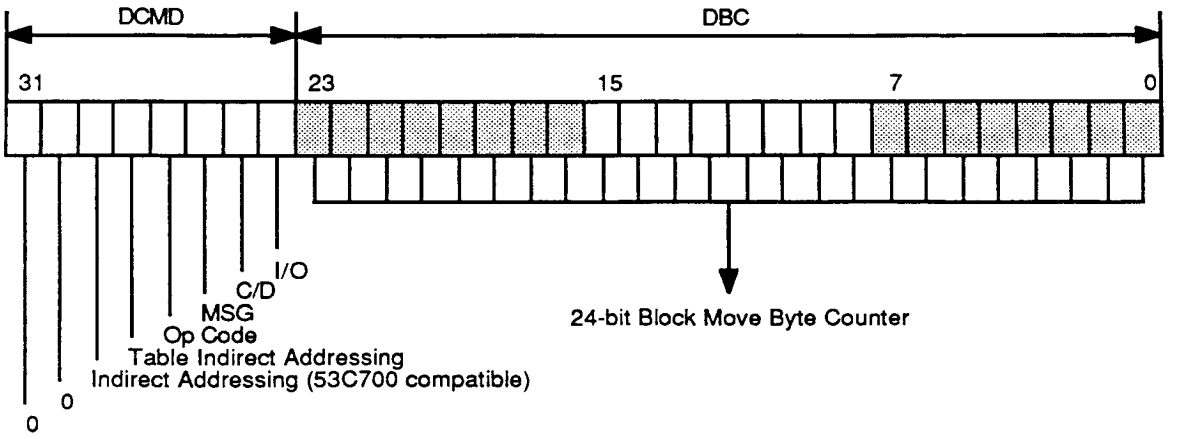
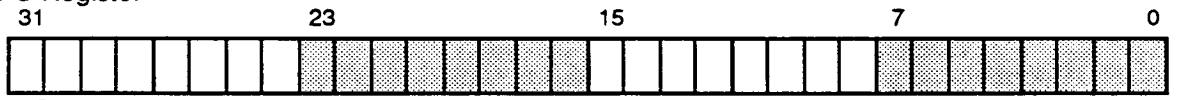
Block Move Instructions



First 32-bit word of the Block Move instruction

DSPS Register



32-bit Start Address of the data to be moved or table entry offset

Second 32-bit word of the Block Move instruction

Bit 29 Indirect Addressing

When this bit is cleared, user data is moved to/from the 32-bit data start address for the Block Move instruction. The value is loaded into the chip's address register and incremented as data is transferred.

When set, the 32-bit user data start address for the Block Move is the address of a pointer to the actual data buffer address. The value at the 32-bit start address is loaded into the chip's DNAD register via a third long word fetch (four byte transfer across the host computer bus).

- Direct -- use the byte count and absolute address in the command.

Command	Byte Count
Address of Data	

- Indirect -- use the byte count in the command and fetch the data address from the address in the command. This feature preserves compatibility with the 53C700.

Command	Byte Count
Address of Address of Data	

Once the data buffer address is loaded, it is executed as if the chip operates in the direct Mode. This indirect feature allows a table of data buffer addresses to be specified. Using the NCR SCSI SCRIPTs compiler, the table offset is placed in the script at compile time. Then at the actual data transfer time, the offsets are added to the base address of the data address table by the external processor. The logical I/O driver builds a structure of addresses for an I/O rather than treating each address individually. This feature makes it possible to locate SCSI SCRIPTs in a PROM.

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Bit 28 Table Indirect

When this bit is set, the 24-bit signed value in the start address of the move is treated as a relative displacement from the value in the DSA Register. Both the transfer count and the source/destination address are fetched from this address.

- Table Indirect -- use the signed integer offset in bits 23-0 of the second 4 bytes of the instruction to fetch first the byte count and then data address. The signed value is combined with the data structure base address to generate the physical address used to fetch values from the data structure.

Command	Not Used
	Table Offset

Prior to the start of an I/O the Data Structure Base Address register (DSA) must be loaded with the base address of the I/O data structure. The address may be any long word on a long word boundary

At the start of an I/O, the DSA is added to the 24-bit signed offset value from the opcode to generate the address of the required data; both positive and negative offsets are allowed. A subsequent fetch from the address brings the data values into the chip.

For a MOVE command, the 24-bit byte count is fetched from system memory. Then the 32-bit physical address is brought into the 53C710. At this point, execution begins.

SCRIPTs can directly execute operating system I/O data structures, saving time at the beginning of an I/O operation. The I/O data structure can begin on any longword boundary and can cross system segment boundaries.

There is one restriction on the placement of data in system memory: The 8 bytes of data in the MOVE command must be contiguous, as shown below. Indirect data fetches are not available during execution of a Memory-to-Memory DMA operation.

(00)	byte count
Physical data address	

Bit 27 Op Code

This 1-bit field defines the instruction to be executed. The Op Code Field bit has different meaning depending on whether the 53C710 is operating in initiator or target Mode. A value not valid for the current operating mode will cause an Illegal Instruction interrupt.

Target Mode

OPC	Instruction Defined
0	MOVE
1	Reserved

1) The 53C710 verifies that it is connected to the SCSI bus as an target before executing this instruction.

2) The 53C710 asserts the SCSI Phase signals (MSG/, C/D, & I/O) as defined by the Phase Field bits in the instruction.

3) If the instruction is for the Command Phase, the 53C710 receives the first command byte and decodes its SCSI Group Code.

   If the SCSI Group Code is either Group 0, Group 1, Group 2, or Group 5, then the 53C710 overwrites the DBC register with the length of the Command Descriptor Block: 6, 10, or 12 bytes.

   If any other Group code is received, the DBC register is not modified and the 53C710 will request the number of bytes specified in the DBC register. If the DBC register contains 000000h an illegal instruction Interrupt is generated.

4) The 53C710 transfers the number of bytes specified in the DBC register starting at the address specified in the DNAD register.

5) If the SCSI ATN/ signal is asserted by the initiator or a parity error occurred during the transfer, the transfer can optionally be halted and an interrupt generated. The Disable Halt on Parity Error or ATN bit in the SXFER register controls whether an interrupt will be generated.

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Initiator Mode

OPC	Instruction Defined
0	Reserved
1	MOVE

1) The 53C710 verifies that it is connected to the SCSI bus as an initiator before executing this instruction.

2) The 53C710 waits for an unserviced phase to occur. An unserviced phase is defined as any phase (with REQ/ asserted) for which the 53C710 has not yet transferred data by responding with an ACK/.

3) The 53C710 compares the SCSI phase bits in the DCMD register with the latched SCSI phase lines stored in the SSTAT2 register. These phase lines are latched when REQ/ is asserted.

4) If the SCSI phase bits match the value stored in the SSTAT2 register, the 53C710 will transfer the number of bytes specified in the DBC register starting at the address pointed to by the DNAD register.

5) If the SCSI phase bits do not match the value stored in the SSTAT2 register, the 53C710 generates a phase mismatch interrupt and the command is not executed.

Bits 26-24 SCSI Phase

This three bit field defines the desired SCSI information transfer phase. When the 53C710 operates in initiator Mode, these bits are compared with the Latched SCSI phase bits in the SSTAT2 register. When the 53C710 operates in target Mode, the 53C710 asserts the phase defined in this field. The following table describes the possible combinations and the corresponding SCSI phase.

MSG	C/D	I/O	SCSI Phase
0	0	0	Data Out
0	0	1	Data In
0	1	0	Command
0	1	1	Status
1	0	0	Reserved Out
1	0	1	Reserved In
1	1	0	Message Out
1	1	1	Message In

Bits 23-0 Transfer Counter

A twenty-four bit field specifying the number of data bytes to be moved between the 53C710 and system memory. The field is stored in the DBC register. When the 53C710 transfers data to/from memory, the DBC register is decremented by the number of bytes transferred. In addition, the DNAD register is incremented by the number of bytes transferred. This process is repeated until the DBC register has been decremented to zero. At that time, the 53C710 fetches the next instruction.

Bits 31-0 Start Address

This 32-bit field specifies the starting address of the data to be moved to/from memory. The field is stored in the DNAD register. When the 53C710 transfers data to/from memory, the DNAD register is incremented by the number of bytes transferred.

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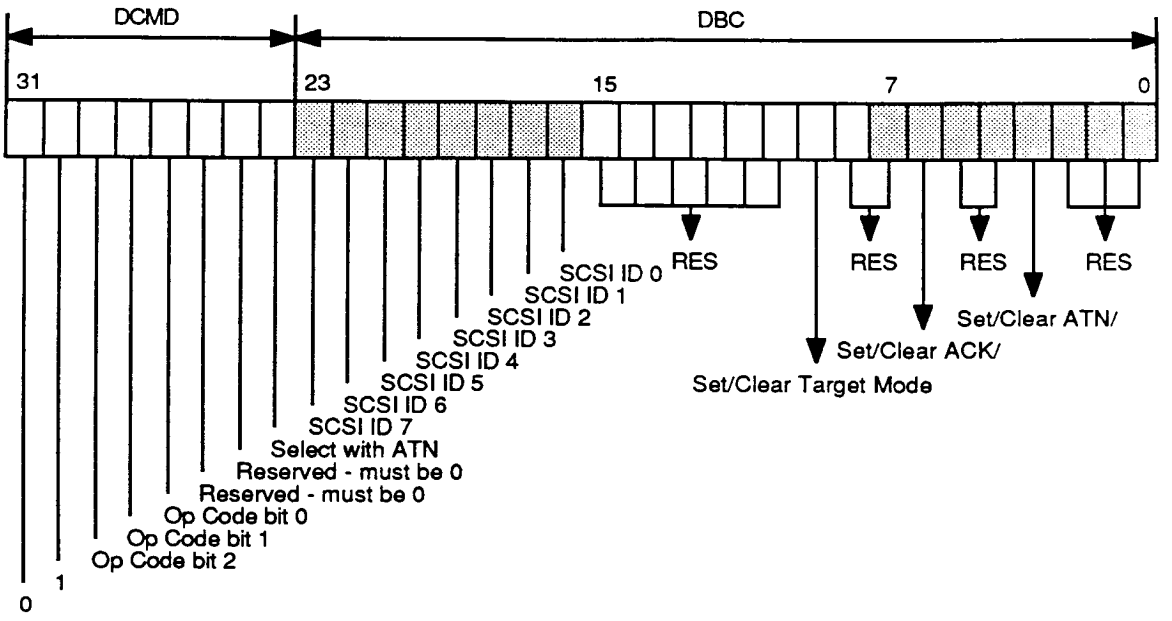
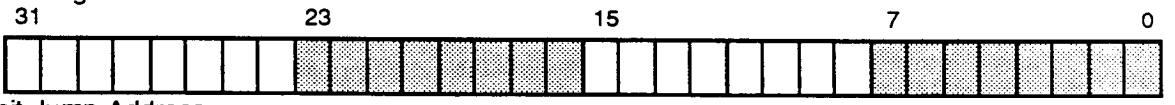
I/O Instructions



First 32-bit word of the I/O instruction

DSPS Register



32-bit Jump Address

Second 32-bit word of the I/O instruction

Bits 29-27 Op Code

The Op Code Field bits have different meanings, depending on whether the 53C710 is in initiator or target Mode. Op Code values 5 through 7 are not reserved, but are considered Read/Write instructions, not I/O, and are discussed in that section.

Target Mode

OPC2	OPC1	OPC0	Instruction Defined
0	0	0	RESELECT
0	0	1	DISCONNECT
0	1	0	WAIT SELECT
0	1	1	SET
1	0	0	CLEAR

RESELECT Instruction

1) The 53C710 arbitrates for the SCSI bus by asserting the SCSI ID stored in the SCID register. If the 53C710 loses arbitration, then it tries again during the next available arbitration cycle without reporting any lost arbitration status.

2) If the 53C710 wins arbitration, it attempts to reselect the SCSI device whose ID is defined in the Destination ID field of the instruction. Once the 53C710 has won arbitration, it fetches the next instruction from the address pointed to by the DSP register.

3) If the 53C710 gets selected or reselected before winning arbitration, it fetches the

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next instruction from the address pointed to by the 32-bit jump address field stored in the DNAD register. The 53C710 automatically configures itself to be in the initiator Mode if reselected, or the target Mode if selected.

DISCONNECT Instruction

1) The 53C710 disconnects from the SCSI bus by deasserting all SCSI signal outputs. The SCSI direction control signals are deasserted which disables the differential pair output drivers.

WAIT SELECT Instruction

1) If the 53C710 is selected, it fetches the next instruction from the address pointed to by the DSP register.

2) If reselected, the 53C710 fetches the next instruction from the address pointed to by the 32-bit jump address field stored in the DNAD register. The 53C710 automatically configures into initiator Mode when reselected.

3) If the CPU sets the SIGP bit in the ISTAT register, the 53C710 will abort the WAIT SELECT instruction and fetch the next instruction from the address pointed to by the 32-bit jump address field stored in the DNAD register.

SET Instruction

1) When the ACK/, ATN/, or target bits are set, the corresponding bits in the SOCL register are set. ACK/ or ATN/ should not be set except for testing purposes.

CLEAR Instruction

1) When the ACK/, ATN/, or target bits are set, the corresponding bits are cleared in the SOCL register. ACK/ or ATN/ should not be set except for testing purposes.

Initiator Mode

OPC2	OPC1	OPC0	Instruction Defined
0	0	0	SELECT
0	0	1	WAIT DISCONNECT
0	1	0	WAIT RESELECT
0	1	1	SET
1	0	0	CLEAR

SELECT Instruction

1) The 53C710 arbitrates for the SCSI bus by asserting the SCSI ID stored in the SCID register. If the 53C710 loses arbitration, it tries again during the next available arbitration cycle without reporting any lost arbitration status.

2) If the 53C710 wins arbitration, it attempts to select the SCSI device whose ID is defined in the instruction's Destination ID field. It then fetches the next instruction from the address pointed to by the DSP register.

3) If the 53C710 is selected or reselected before winning arbitration, it fetches the next instruction from the address pointed to by the 32-bit jump address field stored in the DNAD register. The 53C710 automatically configures itself to initiator Mode if it was reselected, or to target Mode if it was selected.

4) If the Select with ATN/ field is set, the ATN/ signal is asserted during the selection phase.

WAIT DISCONNECT Instruction

1) The 53C710 waits for the target to perform a "legal" disconnect from the SCSI bus. A "legal" disconnect occurs when BSY/ and SEL/ are inactive for a minimum of a Bus Free Delay (400 ns), after the 53C710 has received a Disconnect Message or a Command Complete Message.

WAIT RESELECT Instruction

1) If the 53C710 is selected before being reselected, it fetches the next instruction from the address pointed to by the 32-bit jump address field stored in the DNAD register. The 53C710 automatically

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configures itself to be in target Mode when selected.

2) If the 53C710 is reselected, it fetches the next instruction from the address pointed to by the DSP register.

3) If the CPU sets the SIGP bit in the ISTAT register, the 53C710 will abort the WAIT RESELECT instruction and fetch the next instruction from the address pointed to by the 32-bit jump address field stored in the DNAD register.

SET Instruction

1) The appropriate bit (ACK/ or ATN/) is set in the SOCL register.

CLEAR Instruction

1) The appropriate bit (ACK/ or ATN/) is cleared in the SOCL register.

Bit 26 Relative addressing Mode

When this bit is set, the 24-bit signed value in the DNAD Register is used as a relative displacement form the current DSP address.

This bit should only be used in conjunction with the select, reselect, wait select, and wait reselect instructions. The Select and Reselect instructions can contain an alternate jump address (absolute) or a relative transfer address.

Bit 25 Table Indirect Mode

When this bit is set, the 24-bit signed value in the DBC Register is used as an offset relative from the value in the DSA Register. The SCSI ID, synchronous offset and synchronous period are loaded from this address.

Prior to the start of an I/O the Data Structure Base Address register (DSA) must be loaded with the base address of the I/O data structure. The address may be any long word on a long word boundary

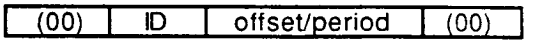
At the start of an I/O, the DSA is added to the 24-bit signed offset value from the opcode to generate the address of the required data; both positive and negative offsets are allowed. A subsequent fetch from the address brings the data values into the chip.

SCRIPTs can directly execute operating system I/O data structures, saving time at the beginning of an I/O operation. The I/O data structure can begin on any longword boundary and can cross system segment boundaries.

There are two restrictions on the placement of data in system memory.

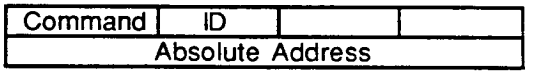
1) The I/O data structure must lie within the 8 MBytes above or below the base address.

2) An I/O command structure must have all four bytes contiguous in system memory, as shown below. The offset/period bits are ordered as in the SXFER register.

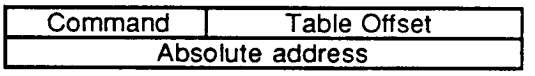


This bit should only be used in conjunction with the select, reselect, wait select, and wait reselect instructions. Bits 1 and 2 may be set individually or in combination:

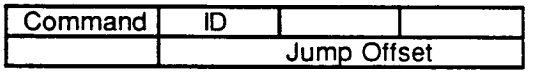
- Direct -- uses the device I.D. and physical address in the command.



- Table Indirect -- uses the physical jump address, but fetches data using the table indirect method.



- Relative -- uses the device I.D. in the command, but treats the alternate address as a relative jump.



- Table Relative-- treats the alternate jump address as a relative jump and fetches the device I.D., Synchronous offset, and Synchronous period indirectly. Adds the

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value in bits 23-0 of the first 4 bytes of the SCRIPT to the data structure base address to form the fetch address.

Command	Table Offset
	Jump Offset

Bit 24 Select with ATN/

This bit specifies whether ATN/ was asserted during the selection phase when the 53C710 is executing a SELECT instruction. When operating in initiator Mode, set this bit for the SELECT instruction. If this bit is set on any other I/O instruction, an illegal instruction interrupt is generated.

Bits 23-16 SCSI Destination ID

This eight bit field specifies the destination SCSI ID for an I/O instruction. Set only one bit in this field.

Bit 9 SET/CLEAR Target Mode

This bit is used in conjunction with a SET or CLEAR command to set or clear target mode. Setting this bit with a SET command configures the 53C710 as a target device (this sets bit 0 of the SCNTL0 register). Setting this bit with a CLEAR command configures the 53C710 as an initiator device (this clears bit 0 of the SCNTL0 register).

Bit 6 SET/CLEAR ACK/

Bit 3 SET/CLEAR ATN/

These two bits are used in conjunction with a SET or CLEAR command to assert or deassert the corresponding SCSI control signal. Bit 6 controls the SCSI ACK/ signal; bit 3 controls the SCSI ATN/ signal.

Setting either of these bits will set or reset the corresponding bit in the SOCL register, depending on the command used. The SET command is used to assert ACK/ and/or ATN/ on the SCSI bus. The CLEAR command is used to deassert ACK/ and/or ATN/ on the SCSI bus.

Since ACK/ and ATN/ are initiator signals, they will not be asserted on the SCSI bus unless the 53C710 is operating as an initiator or the SCSI Loopback Enable bit is set in the CTEST4 register.

The SET/CLEAR SCSI ACK/ATN instruction would be used after message phase Block Move operations to give the initiator the opportunity to assert attention before acknowledging the last message byte. For example, if the initiator wishes to reject a message, an ASSERT SCSI ATN instruction would be issued before a CLEAR SCSI ACK instruction. After the target has serviced the request for a message-out phase, ATN is deasserted with a CLEAR SCSI ATN instruction.

Bits 31-0 Jump Address

This thirty-two bit field specifies the address of the instruction to fetch when the 53C710 encounters a jump condition. The 53C710 fetches instructions from the address pointed to by this field whenever the 53C710 encounters a SCSI condition that is different from the condition specified in the instruction.

For example, during the execution of a SELECT instruction in initiator Mode, if the 53C710 is reselected, then the next instruction is fetched from the address pointed to by the jump address field. For a complete description of the different jump conditions, refer to the description of each instruction.

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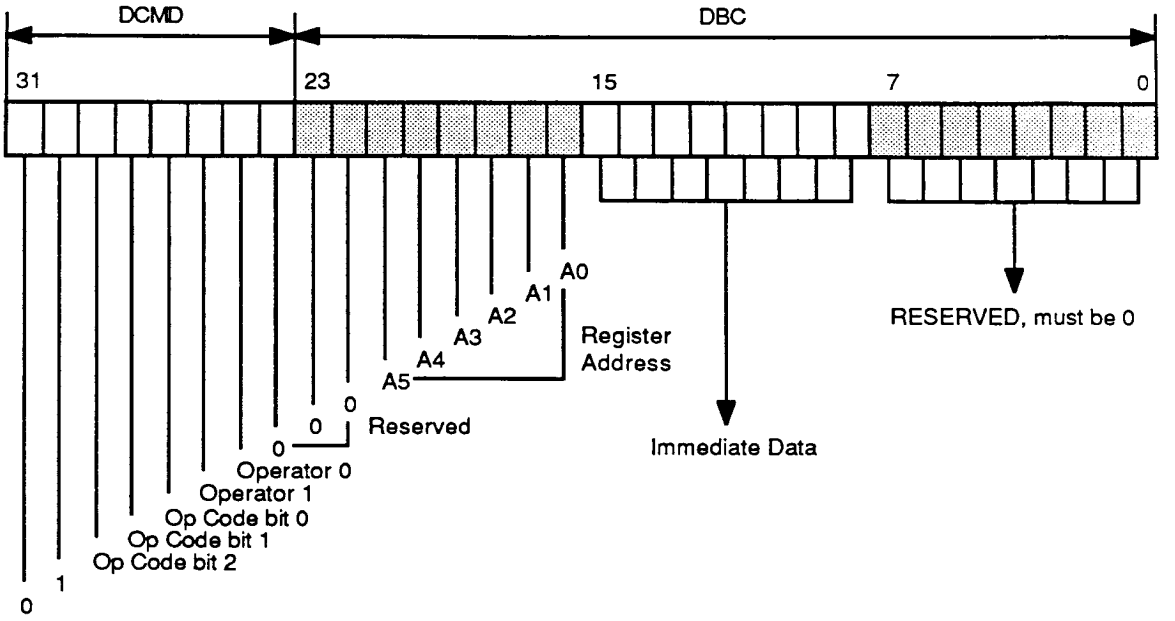
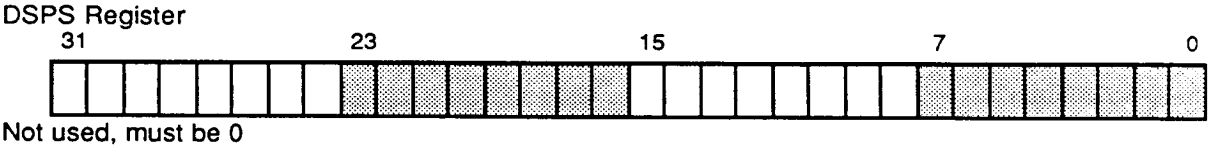
Read/Write Instructions



First 32-bit word of the Read/Write Register Instructions



Second 32-bit word of the Read/Write Register Instructions

Operator	Opcode 7 (111) Read modify Write	Opcode 6 (110) Move to SFBR	Opcode 5 (101) Move from SFBR
00	Immediate data to destination register	Immediate data to SFBR	Immediate data to destination register
01	Immediate data OR'ed with destination register	Immediate data OR register to SFBR	Immediate data OR'ed with SFBR to destination register
10	Immediate data AND'ed with destination register	Immediate data AND register to SFBR	Immediate data AND'ed with SFBR to destination register
11	Immediate data added to destination register	Immediate data added with register to SFBR	Immediate data added with SFBR to destination register

Bits 21-16 A(5:0) - Register Address

Registers values may be changed from SCRIPTs in read-modify-write cycles or move to/from SFBR cycles. A(5:0) select an 8-bit source/destination register within the 53C710. Register addresses are always little endian addresses.

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Read-Modify-Write

The register is read, the selected operation is performed, and the result is written back to the source register.

The Add operation can be used to increment or decrement register values (or memory values if used in conjunction with a memory-to-register move operation) for use as loop counters.

Move to/from SFBR

All operations are read-modify-writes. However, two registers are involved, one of which is always the SFBR.

- Write one byte (value contained within the SCRIPT instruction) into any chip register.
- Move to/from the SFBR from/to any other register.
- Alter the value of a register with And/Or/Add operators.

After moving in values to SFBR, the compare and jump, call, etc commands may be used to check the value.

A Move-to-SFBR followed by a Move-from-SFBR can be used to perform a register to register move.

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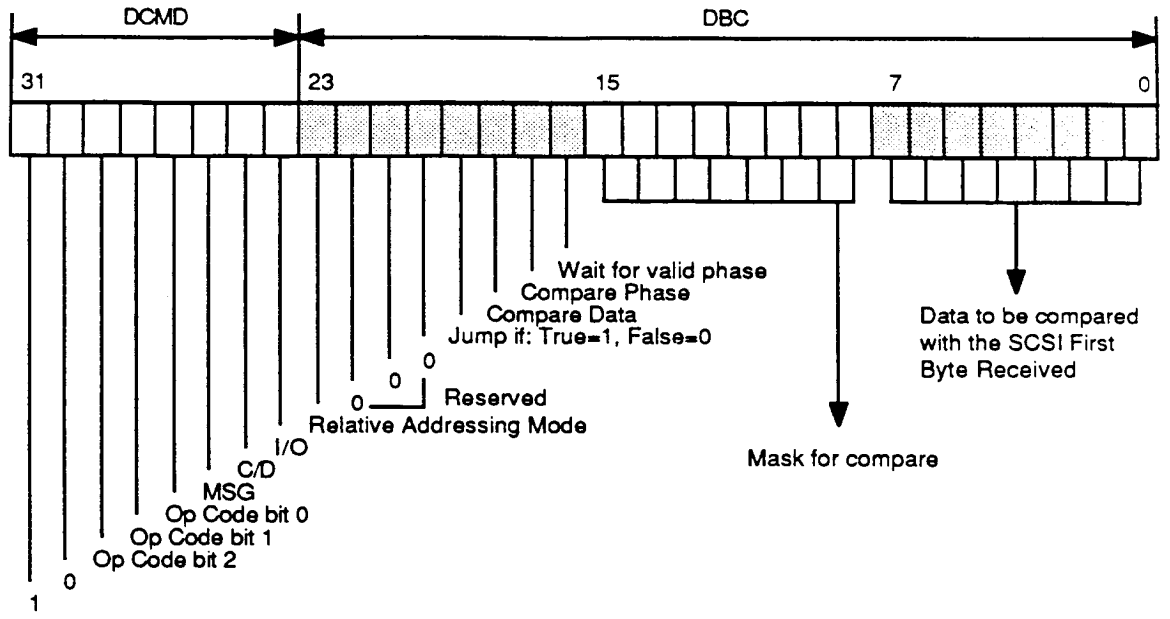
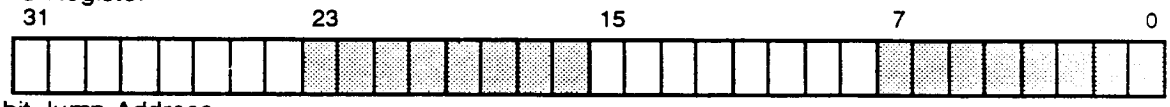
Transfer Control Instructions



First 32-bit word of the Transfer Control instructions

DSPS Register



32-bit Jump Address

Second 32-bit word of the Transfer Control instructions

Bits 29-27 Op Code

This 3-bit field specifies the type of transfer control instruction to be executed. All transfer control instructions can be conditional. They can be dependent on a comparison of the SCSI information transfer phase with the Phase Field and/or a comparison of the First Byte Received with the Data Compare Field. Each instruction can operate in initiator or target Mode.

OPC2	OPC1	OPC0	Instruction Defined
0	0	0	JUMP
0	0	1	CALL
0	1	0	RETURN
0	1	1	INTERRUPT
1	X	X	Reserved

JUMP Instruction

1) The 53C710 compares the phase and/or data as defined by the Phase Compare, Data Compare and True/False bit fields. If the comparisons are true, the 53C710 loads the DSP register with the contents of the DSPS register. The DSP register now contains the address of the next instruction.

2) If the comparisons are false, the 53C710 fetches the next instruction from the address pointed to by the DSP register leaving the instruction pointer unchanged.

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CALL Instruction

1) The 53C710 compares the phase and/or data as defined by the Phase Compare, Data Compare, and True/False bit fields. If the comparisons are true, the 53C710 loads the DSP register with the contents of the DSPS register and that address value becomes the address of the next instruction.

   When the 53C710 executes a CALL instruction, the instruction pointer contained in the DSP register is stored in the TEMP register.

   When a RETURN instruction is executed, the value stored in the TEMP register is returned to the DSP register.

2) If the comparisons are false, the 53C710 fetches the next instruction from the address pointed to by the DSP register and the instruction pointer is not modified.

Note: The Memory Move instruction destroys the return address stored in the TEMP Register.

RETURN Instruction

1) The 53C710 compares the phase and/or data as defined by the Phase Compare, Data Compare, and True/False bit fields. If the comparisons are true, then the 53C710 loads the DSP register with the contents of the DSPS register. That address value becomes the address of the next instruction.

   When the 53C710 executes a CALL instruction, the current instruction pointer contained in the DSP register is stored in the TEMP register.

   When a RETURN instruction is executed, the value stored in the TEMP register is returned to the DSP register.

   The 53C710 does not check to see whether the CALL instruction has already been executed. It will not generate an an interrupt if a RETURN instruction is executed without previously executing a CALL instruction.

2) If the comparisons are false, then the 53C710 fetches the next instruction from the address pointed to by the DSP register and the instruction pointer will not be modified.

Note: The Memory Move instruction destroys the return address stored in the TEMP Register.

INTERRUPT Instruction

1) The 53C710 compares the phase and/or data as defined by the Phase Compare, Data Compare, and True/False bit fields. If the comparisons are true, then the 53C710 generates an interrupt by asserting the IRQ/ signal.

2) The 32-bit address field stored in the DSPS register (not DNAD as in 53C700) can contain a unique interrupt service vector. When servicing the interrupt, this unique status code allows the ISR to quickly identify the point at which the interrupt occurred.

3) The 53C710 halts and the DSP register must be written to start any further operation.

Bits 26-24 SCSI Phase

This three bit field corresponds to the three SCSI bus phase signals which is compared with the phase lines latched when REQ/ is asserted. Comparisons can be performed to determine the SCSI phase actually being driven on the SCSI bus. The following table describes the possible combinations and their corresponding SCSI phase. These bits are only valid when the 53C710 is operating in initiator Mode; when the 53C710 is operating in the target Mode, these bits should be cleared.

MSG	C/D	I/O	SCSI Phase
0	0	0	Data Out
0	0	1	Data In
0	1	0	Command
0	1	1	Status
1	0	0	Reserved Out
1	0	1	Reserved In
1	1	0	Message Out
1	1	1	Message In

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Bit 23 Relative Addressing Mode

When this bit is set, the 24-bit signed value in the DSPS Register is used as a relative offset from the current DSP address (which is pointing to the next instruction, not the one currently executing). Relative Mode does not apply to Return and Interrupt SCRIPTs.

- Jump/Call an absolute address -- start execution at the new absolute address.

Command	Condition Codes
Absolute Address	

- Jump/Call a relative address -- start execution at the current address plus (or minus) the relative offset.

Command	Condition Codes
	Jump Offset

The SCRIPTs program counter is a 32-bit value pointing to the SCRIPT currently being executed by the 53C710. The next address is formed by adding the 32-bit program counter to the 24 bit signed value of the last 24 bits of the Jump or Call instruction. Because it is signed (two's compliment), the jump can be forward or backward.

A relative transfer can be to any address within an 16 MByte segment. The program counter is combined with the 24-bit signed offset (using addition or subtraction) to form the new execution address.

SCRIPTs programs may have any mixture of direct jumps and relative jumps to provide maximum versatility in writing SCRIPTs. For example, major sections of code can be accessed with a far or direct call using the 32-bit physical address, then local labels can be called using a relative transfer.

Executing a SCRIPT requires the driver to load the entry point into the chip with no further intervention if executing entirely in the Relative Jump Mode. A SCRIPT can be created, loaded into a ROM, and executed with no need for any dynamic alternation (patching) of physical addresses at load time.

Bits 22-20 Reserved

Bit 19 Jump If True/False

This bit determines whether the 53C710 should branch when a comparison is true or when a comparison is false. This bit applies to both Phase Compares and Data Compares. If both the Phase Compare and Data Compare bits are set, then both compares must be true to branch on a true condition. Both compares must be false to branch on a false condition.

Bit 19	Compare	Action
0	false	Jump Taken
0	true	No Jump
1	false	No Jump
1	true	Jump Taken

Bit 18 Compare Data

When this bit is set, then the first byte received from the SCSI data bus (contained in SFBR register) is compared with the Data to be Compared Field in the Transfer Control instruction. The Wait for Valid Phase bit controls when this compare will occur. The Jump if True/False bit determines the condition (true or false) to branch on.

Bit 17 Compare Phase

When the 53C710 is in initiator Mode, this bit controls phase compare operations. When this bit is set, the SCSI phase signals (latched by REQ/) are compared to the Phase Field in the Transfer Control instruction; if they match, then the comparison is true. The Wait for Valid Phase bit controls when the compare will occur.

When the 53C710 is operating in target Mode this bit, when set, tests for an active SCSI ATN/ signal.

Bit 16 Wait For Valid Phase

If the Wait for Valid Phase bit is set, then the 53C710 waits for a previously unserviced phase before comparing the SCSI phase & data.

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If the Wait for Valid Phase bit is clear, then the 53C710 compares the SCSI phase & data immediately.

Bits 15-8 Data Compare Mask

The Data Compare Mask allows a SCRIPT to test certain bits within a data byte. During the data compare, any mask bits that are set cause the corresponding bit in the SFBR data byte to be ignored.

For instance, a mask of 01111111b and data compare value of 1XXXXXXXb allows the SCRIPTs processor to determine whether or not the high order bit is on while ignoring the remaining bits.

Bits 7-0 Data Compare Value

This 8-bit field is the data to be compared against the SCSI First Byte Received (SFBR) Register. These bits are used in conjunction with the Data Compare Mask Field to test for a particular data value.

Bits 31-0 Jump Address

This 32-bit field contains the address of the next instruction to fetch when a jump is taken. Once the 53C710 has fetched the instruction from the address pointed to by these 32-bits, this address is incremented by 4, loaded into the DSP register and becomes the current instruction pointer.

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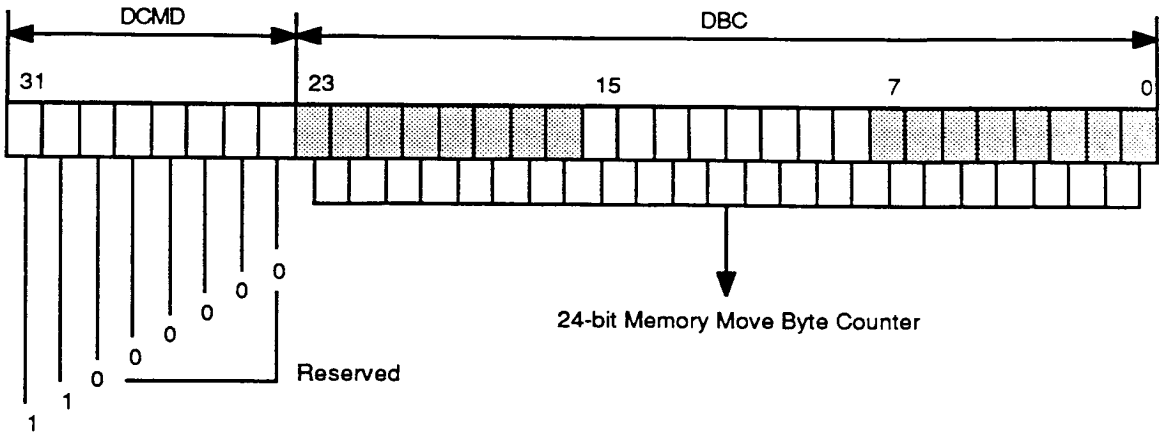
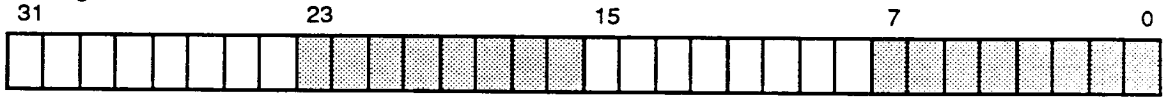
Memory Move Instructions



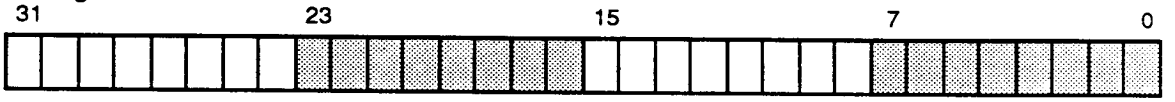
First 32-bit word of the Memory Move instruction

DSPS Register



Second 32-bit word - source address of the Memory Move instruction

TEMP Register



Third 32-bit word - destination address of the Memory Move instruction

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The Memory Move instruction is used to copy the specified number of bytes from the source address to the destination address.

Allowing the 53C710 to perform memory moves frees the system processor for other tasks and moves data at higher speeds than available from current DMA controllers. Up to 16 megabytes may be transferred with one instruction. There are three restrictions:

1) Both the source and destination addresses must start with the same address alignment (A(1:0) must be the same). If source and destination are not aligned, then an illegal instruction interrupt will occur.

2) During execution of this opcode, TEMP and DSA are destroyed. Therefore, if the contents of either register are required for additional SCRIPTs, save them before any Memory Move is executed. Before resuming a SCSI SCRIPT, restore the contents to the appropriate register.

3) Indirect addresses are not allowed.

A special block move instruction passes the source and destination addresses and the byte count to the 53C710. A burst of data is fetched from the source address, put into the DMA FIFO and then written out to the destination address. The move continues until the byte count decrements to zero, then another SCRIPT is fetched from system memory.

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Upon completion of the move, an interrupt instruction or jump to a SCSI function should be executed. The Memory Move instruction invalidates any return address currently stored in the chip.

The DSPS and DSA registers used as additional holding registers used during the Memory Move.

Bits 29-24 Reserved

These bits are reserved and must be zero. If any of these bits is set, an illegal instruction interrupt will occur.

Bits 23-0 Transfer Count

The number of bytes to be transferred is stored in the lower 24 bits of the first instruction word.

Read/Write System Memory from a Script

By using the Memory Move instruction, single or multiple register values may be transferred to/from system memory.

Because the Chip Select (CS/) input is derived from an address decode, it could activate during a Memory Move operation if the source/destination address decoded to within the chips register space. If this occurs, the register pointed to by the lower six bits of the memory address is taken to be the data source or destination. In this way, register values can be saved to system memory and later restored, and SCRIPTs can make decisions based on data values in system memory.

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FUNCTIONAL DESCRIPTION

The 53C710 is composed of three tightly coupled functional blocks: SCSI Core; DMA Core; and SCRIPTs Processor.

SCSI Core

The SCSI core is designed to allow simple migration to SCSI-2 wide bus. It supports synchronous transfer rates of up to 10.0 MBytes/sec, and asynchronous transfer rates greater than 5 MBytes/sec. The programmable SCSI interface makes it easy to "fine tune" the system for specific mass storage devices or SCSI-2 requirements.

The SCSI core offers low level register access or a high-level control interface. Like first generation SCSI devices, the 53C710 SCSI core can be accessed as a register oriented device. The ability to sample and/or assert any signal on the SCSI bus can be used in error recovery and diagnostic procedures. Loopback diagnostics are supported, the SCSI core may perform a self-selection and operate as both an initiator and a target. The 53C710 can test the SCSI pins for physical connection to the board or the SCSI bus.

Unlike previous generation devices, the SCSI core can be controlled by the integrated DMA core through a high-level logical interface. Commands controlling the SCSI core are fetched out of the main host memory. These commands instruct the SCSI core to Select, Reselect, Disconnect, Wait for a Disconnect, Transfer Information, Change Bus Phases and in general, implement all aspects of the SCSI protocol. The SCRIPTs PROCESSOR is a special 2 MIPs processor on the SCSI chip.

DMA Core

The DMA core is a bus master DMA device that directly attaches to 68030 and 68040 processors, and to other processors (80386, 80486, etc.) with minimal logic.

The 53C710 supports 32-bit memory and automatically supports misaligned DMA transfers. A 64 byte FIFO allows the 53C710 to support one, two, four, or eight long words to be burst across the memory bus interface providing memory transfer rates in excess of 66 MBytes/sec. This DMA interface doesn't support dynamic bus sizing.

The DMA core is tightly coupled to the SCSI core through the SCRIPTs PROCESSOR which supports uninterrupted scatter/gather memory operations. A flexible arbitration scheme allows either daisy-chained or wire-OR'ed memory bus request implementations.

SCRIPTs Processor

The SCSI SCRIPTs Processor is a 2 MIPs processor that allows both DMA and SCSI instructions to be fetched from host memory. Algorithms written in SCSI SCRIPTs can control the actions of the SCSI and DMA cores and are executed from 32-bit system memory. Complex SCSI bus sequences are executed independently of the host CPU.

The SCRIPTs Processor can begin a SCSI I/O operation in 500 ns. This compares to 2-8 msec required for traditional intelligent host adapters. The SCRIPTs PROCESSOR offers performance and customized algorithms. Algorithms may be designed to tune SCSI bus performance, to adjust to new bus device types (i.e. scanners, communication gateways, etc.), or to incorporate changes in the SCSI-2/3 logical bus definitions without sacrificing I/O performance.

SCSI SCRIPTs are independent of the CPU and system bus in use.

Big/Little Endian Support

The Big/Little Endian mode select pin gives the 53C710 the flexibility of operating with either byte orientation. Internally, in either mode, the byte lanes of the DMA FIFO and registers are not modified. Because the 53C710 supports only byte and long word slave accesses, the logic required to support both modes is simplified.

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When a long word is accessed, no repositioning of the individual bytes is necessary, since long words are addressed by the address of the least significant byte. Since long words are always used by SCRIPTs, compatibility is maintained.

Big/little has the most effect on byte operations. Internally, the 53C710 adjusts the byte control logic of the DMA FIFO and register decodes to enable the appropriate byte lane. The registers will always appear on the same byte lane, but the address of the register will be repositioned.

Data to be transferred between system memory and the SCSI bus always starts at address zero and continues through address 'n' - there is no byte ordering in the chip. The first byte in from the SCSI bus goes to address 0, the second to address 1, etc. Going out onto the SCSI bus, address zero is the first byte out on the SCSI bus, address 1 is the second byte, etc.

Correct SCRIPTs will be generated if the SCRIPTs compiler is run on a system that has the same byte ordering as the target system. Any SCRIPT patching in memory must patch the instruction in the order that the SCRIPTs processor expects it.

Software drivers for the 53C710 should write to registers by logical name (ie. "SCNTL0"). The logical name should be equated to address 03h in big endian mode and address 00h in little endian mode, so there is no change the software when moving from one mode to the other; only the equate file needs to be changed.

Addressing of registers from within a SCRIPT is independent of bus mode; internally, the 53C710 always operates in little endian mode.

Big Endian Mode

Big Endian is used primarily in Motorola processor based designs. The 53C710 treats D(31:24) as the lowest physical memory address. The register map is left justified (Address 03h = SCNTL0).

Little Endian Mode

Little endian is used primarily in Intel processor based designs. This mode treats D(7:0) as the lowest physical memory address. The register map is right justified (Address 00h = SCNTL0).

System Data Bus	(31:24)	(23:16)	(15:8)	(7:0)
53C710 Pins	(31:24)	(23:16)	(15:8)	(7:0)
Register	SCNTL0	SCNTL1	SDID	SIEN
Big Endian Addr	03h	02h	01h	00h
Little Endian Addr	00h	01h	02h	03h

Loopback Mode

The 53C710 Loopback Mode allows testing of both initiator and target operations and, in effect, lets the chip talk to itself. When the Loopback Enable bit is set in the CTEST4 register, the 53C710 allows control of all SCSI signals, whether the 53C710 is operating in initiator or target Mode. To implement the loopback function, perform the following steps.

1) Set the Loopback Enable bit in the CTEST4 register.

2) Set-up the desired arbitration Mode as defined in the SCNTL0 register.

3) Set the Start Sequence bit in the SCNTL0 register.

4) Poll the SBCL register to determine when SEL/ is active and BSY/ is inactive.

5) Poll the SBDL register to determine which SCSI ID bits are being driven.

6) In response to selection, set the BSY/ bit (bit 5 of the SOCL register).

7) Poll the SEL/ bit in the SBCL register to determine when SEL/ becomes inactive.

8) To assert the desired phase, write the MSG/, C/D, and I/O bits to the desired phase in the SOCL register.

9) To assert REQ/, keep the phase bits the same and set the REQ/ bit in the SOCL register. To accommodate the 400 ns Bus Settle Delay, assert REQ/ after asserting the phase signals.

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10) The initiator role can be implemented by SCSI SCRIPTs. Next issue a Block Move instruction to select the appropriate phase.

The above procedure describes how to perform selection in the SCSI Loopback Mode. There are many sequences that can be tested. Generally, the 53C710 must execute initiator instructions and the host CPU implements the target role by asserting the appropriate SCSI signals and polling for the appropriate SCSI signals.

Parity Checking for Loopback

When the 53C710 is sending data in loopback mode, parity is generated. The parity is checked via bit 1 of the SSTAT1 register when the data is read back.

Parity cannot be generated or checked when the 53C710 is receiving data in loopback Mode.

Parity Options

The 53C710 implements a flexible parity scheme that allows control of the parity sense, allows parity checking to be turned on or off, and has the ability to deliberately send a byte with bad parity over the SCSI bus to test parity error recovery procedures. The following bits are involved in parity control and observation:

1) Assert ATN/ on parity errors - Bit 1 in the SCNTL0 register.

   This bit causes the 53C710 to automatically assert SCSI ATN/ when it detects a parity error while operating as an initiator.

2) Enable Parity Generation - Bit 2 in the SCNTL0 register.

   This bit determines whether the 53C710 generates parity sent to the SCSI bus or allows parity to "flow through" the chip to/from the SCSI bus and system bus.

3) Enable Parity Checking - Bit 3 in the SCNTL0 register.

   This bit enables the 53C710 to check for parity errors. The 53C710 checks for odd or even parity depending on the status of the Assert Even SCSI Parity bit.

4) Assert Even SCSI Parity - Bit 2 in the SCNTL1 register.

   This bit determines the SCSI parity sense checked & generated by the 53C710.

5) Disable Halt on ATN/ or a Parity Error target Mode Only - Bit 7 in SXFER register.

   This bit causes the 53C710 to halt operations when a parity error is detected in target Mode.

6) Enable Parity Error Interrupt - Bit 0 in the SIEN register.

   This bit determines whether the 53C710 will generate an interrupt when it detects a parity error.

7) Parity Error - Bit 0 in the SSTAT0 register.

   This status bit is set whenever the 53C710 has detected a parity error on either the SCSI bus or the system bus.

8) Status of SCSI Parity Signal - Bit 0 in the SSTAT1 register.

   This status bit represents the live SCSI Parity signal (SDP/).

9) Latched SCSI Parity Signal - Bit 3 in the SSTAT2 register.

   This status bit contains the SCSI parity of the byte latched in the SIDL.

10) DMA FIFO Parity bit - Bit 3 in the CTEST2 register.

    This status bit is represents the parity bit in the DMA FIFO after data is read from the FIFO by reading the CTEST6 register.

11) DMA FIFO Parity bit - Bit 3 in the CTEST7 register.

    This write-only bit is written to the DMA FIFO after writing data to the DMA FIFO by writing the CTEST6 register.

12) SCSI FIFO Parity bit - Bit 4 in the CTEST2 register.

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This status bit represents the parity bit in the SCSI FIFO after data is read from the FIFO by reading the CTEST3 register.

Table 3. Parity Control

EPG	EPC	AESP	Description
0	0	0	Will not check for parity errors. Parity flows from DP(3:0) thru the chip to SCSI bus when sending SCSI data, Parity flows from the SCSI bus to DP(3:0) when receiving SCSI data. Asserts odd parity when sending SCSI data.
0	0	1	Will not check for parity errors. Parity flows from DP(3:0) thru the chip to the SCSI bus when sending SCSI data. Parity flows from the SCSI bus to DP(3:0) when receiving SCSI data. Asserts even parity when sending SCSI data.
0	1	0	Checks for odd parity on both SCSI data received and system data when sending. Parity flows from DP(3:0) thru the chip to the SCSI bus when sending SCSI data, Parity flows from SCSI bus to DP(3:0) when receiving SCSI data. Asserts odd parity when sending SCSI data
0	1	1	Checks for even parity on both SCSI data received and system data when sending. Parity flows from DP(3:0) thru the chip to the SCSI bus when sending SCSI data, Parity flows from the SCSI bus to DP(3:0) when receiving SCSI data. Asserts even parity when sending SCSI data.
1	0	0	Will not check for parity errors. Parity on DP(3:0) is ignored. Parity is generated when sending SCSI data. Parity flows from SCSI bus to the chip but is not asserted on DP(3:0) when receiving SCSI data. Asserts odd parity when sending SCSI data.
1	0	1	Will not check for parity errors. Parity on DP(3:0) is ignored. Parity is generated when sending SCSI data. Parity flows from SCSI bus to chip, but is not asserted on DP(3:0) when receiving SCSI data. Asserts even parity when sending SCSI data.
1	1	0	Checks for odd parity on both SCSI data received and system data, when sending. Parity on DP(3:0) is ignored. Parity is generated when sending SCSI data. Parity flows from SCSI bus to the chip, but is not asserted on DP(3:0) when receiving SCSI data. Asserts odd parity when sending SCSI data.
1	1	1	Checks for even parity on both SCSI data received and system data, when sending. Parity on DP(3:0) is ignored. Parity is generated when sending SCSI data. Parity flows from SCSI bus to the chip, but is not asserted on DP(3:0) when receiving SCSI data. Asserts even parity when sending SCSI data

Key: EPG = Enable Parity Generation
EPC = Enable Parity Checking
AESP = Assert SCSI Even Parity

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Parity Errors and Interrupts

This table describes the options available when an parity error occurs. This table only applies to the case where the Enable Parity Checking bit is set.

DHP	EPI	Description
0	0	Will NOT halt when a parity error occurs in target or initiator Mode
0	1	Will interrupt when a parity error occurs in target or initiator Mode
1	0	Will halt when a parity error occurs in target Mode, will NOT generate an interrupt
1	1	Will halt when a parity error occurs in target Mode, will generate an interrupt in target or initiator Mode

Key: DHP Disable Halt on ATN/ or Parity Error
EPI Enable Parity Interrupt

Diagnostics

DMA FIFO Test

The DMA FIFO is more complex than the SCSI FIFO. The DMA FIFO is a 64 X 9 bit FIFO. It can be divided into 4 sections, each being 9-bits wide and 16 transfers deep.

Each of these four sections is called a byte lanes. Each byte lane can be individually tested by writing known data into the FIFO and reading that same data back out of the FIFO.

To write data into the DMA FIFO, load the data 9 bits per instruction. Data is written to the top of the FIFO. Data is read from the bottom of the FIFO. Three control bits in the CTEST4 register allow access to any one of the four "byte lanes."

Parity is written to the FIFO through bit 3 of the CTEST7 register. Set this bit to the desired value before each write operation to the FIFO.

To the appropriate "byte lane", write the following three bits as shown below.

FBL2	FBL1	FBL0	Description
0	X	X	disabled
1	0	0	Byte Lane 0
1	0	1	Byte Lane 1
1	1	0	Byte Lane 2
1	1	1	Byte Lane 3

X = Don't Care

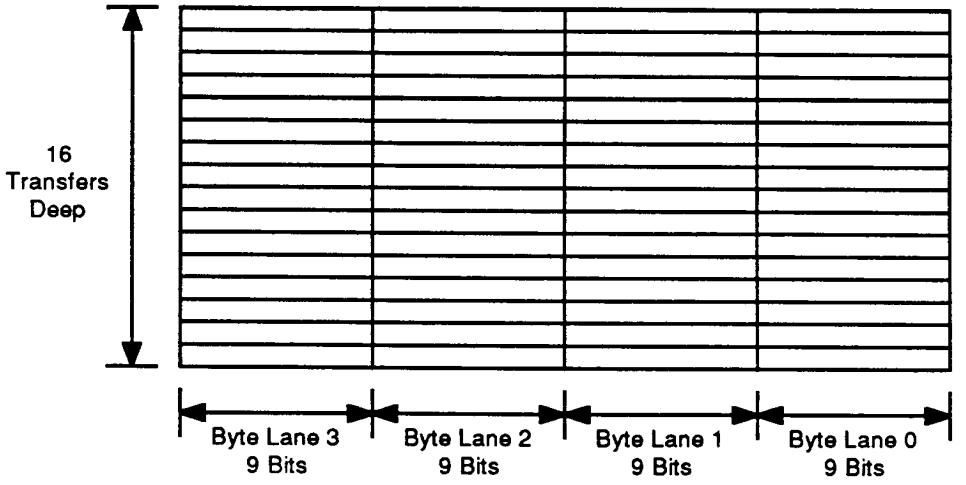

Figure 4. DMA FIFO

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To completely load the DMA FIFO with known data and read back the data parity, perform the following steps.

1) Write an 04h to the CTEST4 register to setup access to Byte Lane zero in the DMA FIFO.

```
outportb(CTEST4,0x04);
```

2) Write the parity bit to the CTEST7 register bit 3 and the 8-bit data value to the CTEST6 register to write the desired data pattern (incrementing) to the DMA FIFO.

```
for(i=0;i<16;++i)
{
outportb(CTEST7,parity);
outportb(CTEST6,i);
}

/* parity values are:
0x08 equals parity of 1
0x00 equals a parity of 0 */
```

3) Read the parity bit in the CTEST2 register to read data back out of the FIFO.

```
for(i=0;i<16;++i)
{
lane0[i]=inportb(CTEST6);
par0[i]=(inportb(CTEST2)&0x08);
}

/* read back in data out of the
FIFO, mask all but the parity
bit -  0x08 = 1
       0x00 = 0 */
```

4) Repeat the above sequence for byte lanes 1 through 3.

5) Disable DMA FIFO access by writing zero to the CTEST4 register.

```
outportb(CTEST4,0x00);
```

SCSI FIFO Test

The SCSI FIFO Write Enable bit in the CTEST4 register is used to load the SCSI Synchronous Data FIFO with data. To load the SCSI FIFO with a known data pattern, set this bit. The data is loaded into the SCSI FIFO by successive writes to the SODL register. The microprocessor reads the CTEST3 register to read data out of the SCSI FIFO. Reading bit 4, the SCSI FIFO parity bit in the CTEST2 register checks parity when reading data out of the FIFO after reading CTEST3. The parity bit is stored in the CTEST2 register during a CTEST3 register read.

Parity can be written to the FIFO in one of two ways.

1) Parity can flow into the 53C710 on the parity signals if the Enable Parity Generation bit in the SCNTL0 register is cleared. The microprocessor drives the parity signal for the corresponding 8-bit data signals.

   For example, writing the FIFO to the 53C710 on "Byte Lane 2" (D(23:16)) should make DP2 drive the parity information.

2) If the Parity Generation bit is set, then the 53C710 forces the parity bit to even or odd parity. Clear the Assert Even SCSI parity bit in the SCNTL1 register to load the SCSI FIFO with odd parity. If this bit is set, then the SCSI FIFO will be loaded with even parity.

   Follow the steps below to completely load the SCSI FIFO with known data and be able to read back the data parity.

a) Write the control bits to determine the loading method and parity sense to be loaded into the SCSI FIFO (see table).

```
outportb(SCNTL0,config0_info);
outportb(SCNTL1,config1_info);
```

b) Set the SCSI FIFO write Enable bit in the CTEST4 register to enable the SCSI FIFO to accept data. When the FIFO test is complete, clear this bit.

```
outportb(CTEST4,0x08);
```

c) Load the SCSI FIFO with the desired data value by writing a known data pattern (incrementing) to the SODL register.

```
for(i=0;i<16;++i)
{
outportb(SODL,i);
}
```


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d) Read the data back by reading the CTEST3 register.

```
for(i=0;i<16;++i)
{
data_in[i]=inportb(CTEST3);
parity_in[i]=inportb(CTEST2);
}

/* should be the incrementing
pattern. Bit 4 of this register
is the parity bit for the byte
just read out of CTEST3 */
```

e) Reset the SCSI FIFO Write Enable bit.

```
outportb(CTEST4,0x00);
```

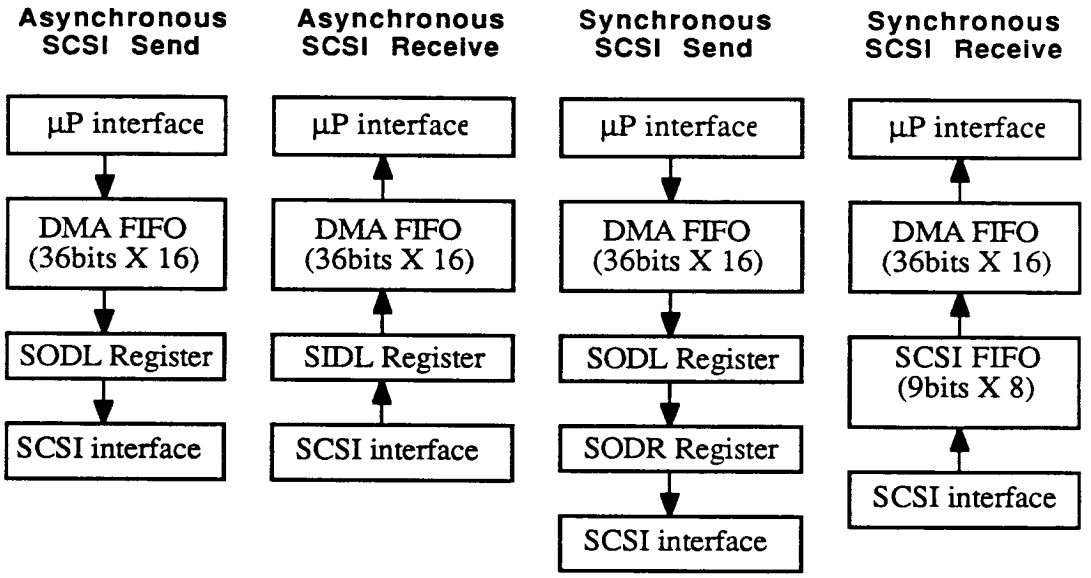
EPG	AESP	Parity sense & loading method
0	X	Parity is loaded on the hardware signals DP(3:0)
1	0	Odd parity is automatically loaded when the SODL register is written
1	1	Even parity is automatically loaded when the SODL register is written

Key: EPG Enable Parity Generation bit (SCNTL0)
AESP Assert Even SCSI Parity bit (SCNTL1, bit 2)
X Don't Care

Host Interface

The data path through the 53C710 is dependent on whether data is being moved into or out of the chip, and whether SCSI data is being transferred asynchronously or synchronously.

The diagrams below show how data is moved to/from the SCSI bus in each of the different modes.



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The following steps will determine if any bytes remain in the data path when the chip halts an operation:

Asynchronous SCSI Send:

1) Use the algorithm described in the DFIFO register description to determine if any bytes are left in the DMA FIFO.

2) Read the SSTAT1 register and examine bit 6 to determine if any bytes are left in the SODL register. If bit 6 is set, then there is a byte in the SODL register.

Synchronous SCSI Send:

1) Use the algorithm described in the DFIFO register description to determine if any bytes are left in the DMA FIFO.

2) Read the SSTAT1 register and examine bit 6 to determine if any bytes are left in the SODL register. If bit 6 is set, then there is a byte in the SODL register.

3) Read the SSTAT1 register and examine bit 5 to determine if any bytes are remaining in the SODR register. If bit 5 is set, then there is a byte in the SODR register.

Asynchronous SCSI Receive:

1) Use the algorithm described in the DFIFO register description to determine if any bytes are left in the DMA FIFO.

2) Read the SSTAT1 register and examining bit 7 to determine if any bytes are left in the SIDL register. If bit 7 is set, then there is a byte in the SIDL register.

Synchronous SCSI Receive:

1) Use the algorithm described in the DFIFO register description to determine if any bytes are left in the DMA FIFO.

2) Read the SSTAT2 register and examine bits 7-4, the binary representation of the number of valid bytes in the SCSI FIFO to determine if any bytes are left in the SCSI FIFO.

Misaligned Transfers

The 53C710 accommodates block data transfers beginning or ending on odd byte or odd word addresses. Such transfers are termed "misaligned." An odd byte is defined as an address with A0 = 1; an odd word has A1 = 1.

At the start of a transfer, if address bit A0=1, the 53C710 will line up to an even byte boundary by performing a single byte transfer. Then, if address bit A1=1, the chip will line up to an even word boundary by performing a single word transfer. Once aligned, 32-bit transfers will be performed until lined up to a Cache-Line boundary (A(3:0)=0). Then, Cache-Line bursts will be performed as long as the byte counter is greater than 32.

Level	Transfer
1	Align to next 16-bit word with 8-bit transfer if A0 =1
2	Align to next 32-bit word with 16-bit transfer if A1 = 1
3	Align to next Cache-Line with 32-bit transfers if A(3:0) ≠ 0
4	Perform Cache-Line bursts (16 bytes) each bus ownership

If Cache-Line Burst mode is disabled by the deassertion of CBACK/ or assertion of TBI//, then Non-Cache-Line Burst transfers will be used. The burst length is set by the programmed threshold level.

If the current byte count indicates insufficient length to complete a current level transfer, the level will be reduced until a bus operation is possible. Alignment at the end of a transfer occurs in reverse order.

Note: While aligning to a Cache-Line boundary at the beginning of a block transfer, the 53C710 performs one bus cycle per host bus ownership, ie. the transfer size (width) will not change during the ownership. However, while "cleaning up" at the end of misaligned block transfer, or if cache bursting is disabled, the size may change during a bus ownership.

The 53C710 does not perform 24-bit transfers, making it easily adaptable to public buses (many of which do not allow 24-bit transfers).

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(Re)Select During (Re)Selection

In multi-threaded SCSI I/O environments, it is not uncommon to be selected or reselected while trying to perform selection/reselection. This situation may occur when a SCSI controller (operating in initiator mode) tries to select one target and gets reselected by another. The analogous situation for target devices is being selected while trying to perform a reselection.

The 53C710 can handle this condition in a manner identical to the 53C700, that is auto-switching between initiator and target modes, but the recommended method is to turn auto-switching off.

With auto-switching enabled, regardless of the current operating mode (initiator/target), if the 53C710 becomes reselected while executing a (RE)SELECT instruction, then it will auto-switch to initiator mode. Similarly, if the 53C710 becomes selected while executing a (RE)SELECT instruction, it will auto-switch to target mode.

After the automatic mode switch, the 53C710 fetches the next instruction from the alternate address, pointed to by the DNAD register (the second 32-bit word of the (RE)SELECT instruction).

The recommended method of handling (re)selection during (re)selection is to disable auto-switching and put a SET TARGET instruction at the start of the target SCRIPT (before the WAIT SELECT code).

Synchronous Operation

The 53C710 can transfer synchronous SCSI data in both initiator and target modes. The SXFER register controls both the synchronous offset and the transfer period, and may be loaded by the CPU before SCRIPT execution begins or from within a SCRIPT via a table indirect I/O instruction.

The 53C710 can always receive data at a synchronous transfer period of 80/160 ns (SCSI-2/SCSI-1), regardless of the transfer period used to send data. Therefore, when negotiating for synchronous data transfers, the suggested transfer period is 80/160 ns. Depending on the SCLK frequency, the 53C710 can send synchronous data at periods as short as 80/160ns.

SCSI Interface

The 53C710 can be used in both single-ended and differential applications.

In single-ended Mode, all SCSI signals are active low. The 53C710 contains the open-drain output drivers and can be connected directly to the SCSI bus. Each output is isolated from the power supply to ensure that a powered-down 53C710 has no effect on an active SCSI bus (CMOS "voltage feed-through" phenomenon). Additionally, signal filtering is present at the inputs of REQ/ and ACK/ to increase immunity to signal reflections.

In Differential Mode, the SDIR(7:0), SDIRP, IGS, TGS, RSTDIR, BSYDIR, and SELDIR signals control the direction of external differential-pair transceivers. See Figure 5 for the suggested differential wiring diagram. The wiring diagram shows five 75ALS170 3-channel transceivers and one 75ALS171 3-channel transceiver, though other single and multi-channel devices may be used (DS36954 4-channel transceiver, for instance). The suggested value for the 15 pull-up resistors in the diagram is 680 Ohms.

Terminator Networks

The terminator networks provide the biasing needed to pull inactive signals to an inactive voltage level, and are required for both single ended and differential applications. Terminators must be installed at the extreme ends of the SCSI cable, and only at the ends; no system should ever have more or less than 2 sets of terminators installed and active. SCSI host adapters should provide a means of accommodating terminators. The terminators should be socketed, so that if not needed they may be removed.

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Single ended cables are terminated differently from differential cables. Single ended cables use a 220 Ohm pull-up to the termination power supply (TERM-POWER) line and a 330 Ohm pull-down to GROUND. Differential cables use a 330 Ohm pull-up from "-SIG" to TERM-POWER, a 330 Ohm pull-down from "+SIG" to GROUND, and a 150 Ohm resistor from "-SIG" to "+SIG".

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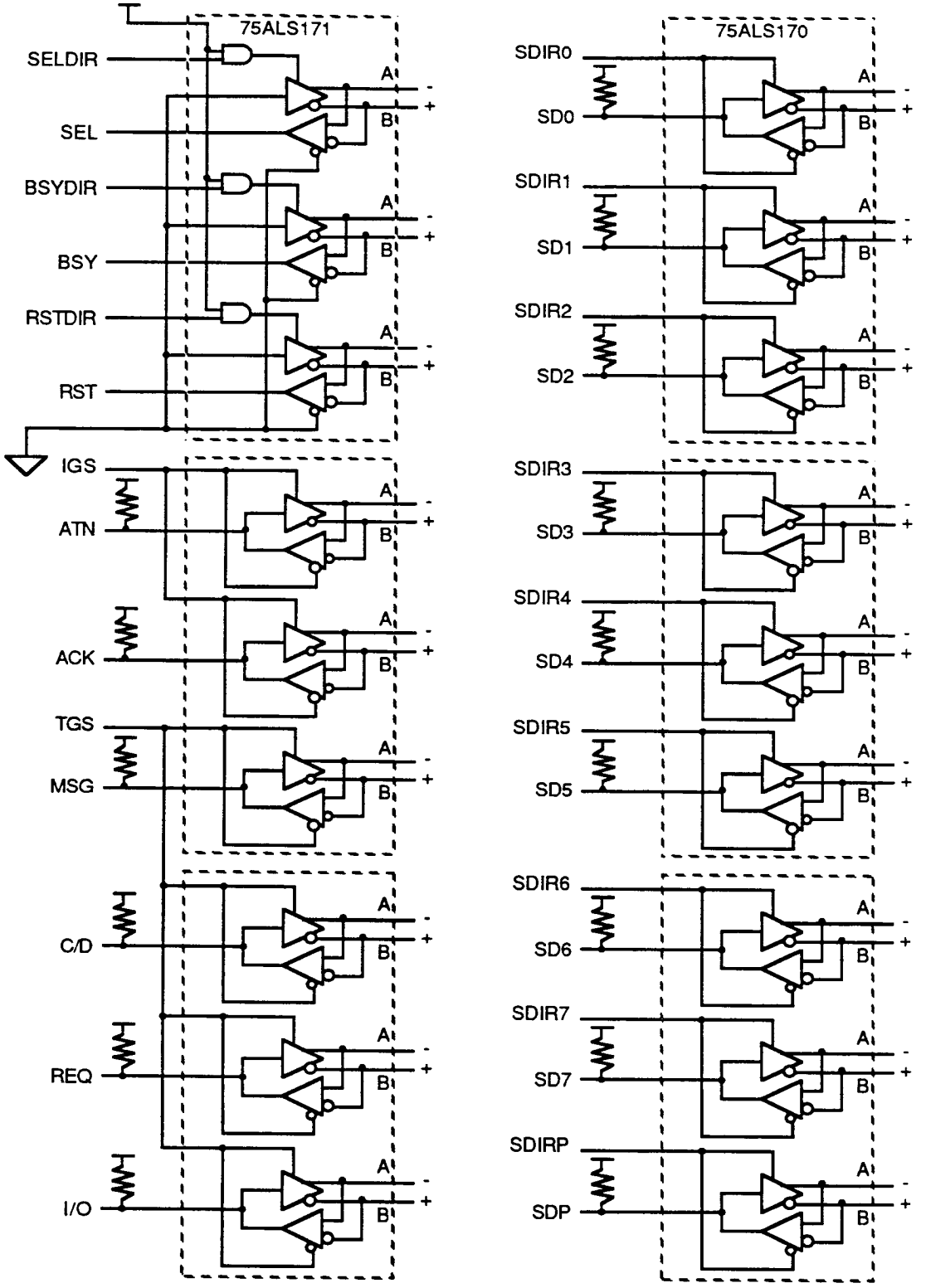
Figure 5. Differential wiring diagram



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DC CHARACTERISTICS

Absolute Maximum Stress Ratings

SYMBOL	PARAMETER	MIN	MAX	UNIT
Tstg	Storage Temperature	-55	150	℃
VDD	Supply Voltage	-0.5	7	V
VIN	Input Voltage	VSS - 0.5	VDD + 0.5	V
ESD*	Electrostatic Discharge	-	4K	V

* SCSI pins only. Tested using the human body model - 100 pF at 1.5 kΩ

Stresses beyond those listed above may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or at any other conditions beyond those indicated in the Operating Conditions section of this specification is not implied.

Operating Conditions

SYMBOL	PARAMETER	MIN	MAX	UNIT
VDD	Supply Voltage	4.75	5.25	V
IDD	Supply Current	-	TBD	mA
Ta	Operating Free-Air	0	70	℃

SCSI Signals - SD(7:0), SDP/, REQ/, MSG/, I/O, C/D, ATN/, ACK/, BSY/, SEL/, RST/

SYMBOL	PARAMETER/ CONDITIONS	MIN	MAX	UNIT
VIH	Input High Voltage	2	VDD + 0.5	V
VIL	Input Low Voltage	VSS - 0.5	0.8	V
VOL	Output Low Voltage IOL = 48 mA	VSS	0.5	V
VHYS	Hysteresis	200		mV
IIN	Input Leakage Current	-10	10	µA
	Input Leakage - SCSI RST	-200	50	µA
IOZ	Three-State Leakage Current	-10	10	µA

Input Signals - BG/, BOFF/, RESET/, CS/, BS, BIG-LIT/, BCLK, SCLK

SYMBOL	PARAMETER/ CONDITIONS	MIN	MAX	UNIT
VIH	Input High Voltage	2	VDD + 0.5	V
VIL	Input Low Voltage	VSS - 0.5	0.8	V
IIN	Input Leakage Current	-1	1	µA

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Output Signals - SDIR(7:0), SDIRP, BSYDIR, SELDIR, RSTDIR, TGS, IGS, BR/, IRQ/

SYMBOL	PARAMETER/ CONDITIONS	MIN	MAX	UNIT
VOH	Output High Voltage IOH = -8 mA	2.4	VDD	V
VOL	Output Low Voltage IOL = 8 mA	VSS	0.4	V
IOH	Output High Current VOH = VDD - 0.5 V	-4	-	mA
IOL	Output Low Current VOL = 0.4 V	8	-	mA

Output Signals - A(31:6), SLACK/, MASTER/, FETCH/

SYMBOL	PARAMETER/ CONDITIONS	MIN	MAX	UNIT
VOH	Output High Voltage IOH = -16 mA	2.4	VDD	V
VOL	Output Low Voltage IOL = 16 mA	VSS	0.4	V
IOH	Output High Current VOH = VDD - 0.5 V	-8	-	mA
IOL	Output Low Current VOL = 0.4 V	16	-	mA

Three-State Output Signals - FC(2:0), SC(1:0), UPSO-TT0/, CBREQ/-TT1/

SYMBOL	PARAMETER/ CONDITIONS	MIN	MAX	UNIT
VOH	Output High Voltage IOH = -16 mA	2.4	VDD	V
VOL	Output Low Voltage IOL = 16 mA	VSS	0.4	V
IOH	Output High Current VOH = VDD - 0.5 V	-8	-	mA
IOL	Output Low Current VOL = 0.4 V	16	-	mA
IOZ	Three-State Leakage Current	-10	10	µA

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Bidirectional Signals - A(5:0), D(31:0), DP(3:0), DS/-DLE, AS/-TS/, R-W/, SIZ(1:0), BERR/-TEA/, HALT/-TIP/, BGACK/-BB/, CBACK/-TBI/, STERM/-TA/

SYMBOL	PARAMETER/ CONDITIONS	MIN	MAX	UNIT
VIH	Input High Voltage	2	VDD + 0.5	V
VIL	Input Low Voltage	VSS - 0.5	0.8	V
VOH	Output High Voltage IOH = -16 mA	2.4	VDD	V
VOL	Output Low Voltage IOL = 16 mA	VSS	0.5	V
IOH	Output High Current VOH = VDD - 0.5 V	-8	-	mA
IOL	Output Low Current VOL = 0.4 V	16	-	mA
IIN	Input Leakage Current	-10	10	µA
IOZ	Three-State Leakage Current	-10	10	µA

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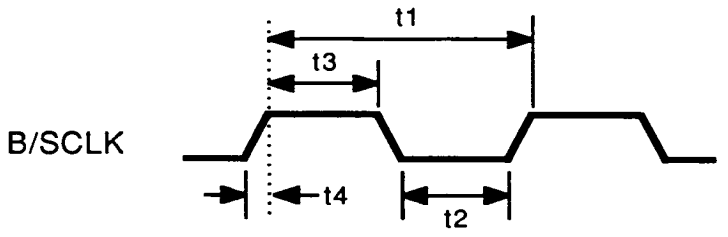
AC CHARACTERISTICS

The AC characteristics described in this section apply over the entire range of operating conditions (see the "DC CHARACTERISTICS" section). Chip timings are based on simulation at worst case voltage, temperature, and processing.

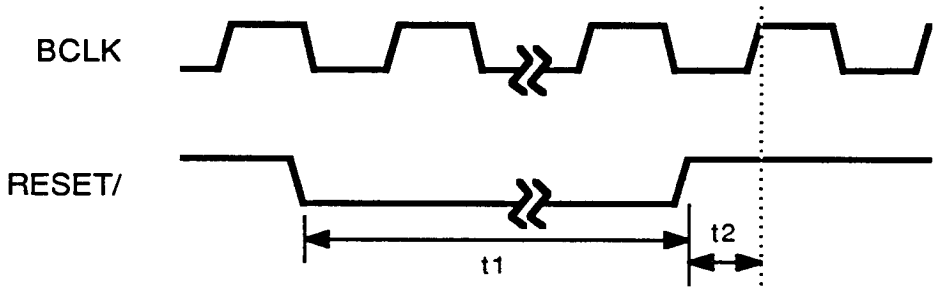
Clock Timing



REF #	PARAMETER	MIN	MAX	UNIT
1	tBCLK - Bus Clock cycle time	30	DC	ns
	tSCLK - SCSI Clock cycle time*	15	60	ns
2	BCLK low time	0.45	0.55	tBCLK
	SCLK low time	0.45	0.55	tSCLK
3	BCLK high time	0.45	0.55	tBCLK
	SCLK high time	0.45	0.55	tSCLK
4	BCLK slew rate	1	-	V/ns
	SCLK slew rate	1	-	V/ns

* This parameter must be met to insure SCSI timings are within specification.

Chip Reset Timing



REF #	PARAMETER	MIN	MAX	UNIT
1	Reset pulse width	10	-	tBCLK
2	Reset deasserted setup to BCLK high	10	-	ns

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Asynchronous Slave Read /Write Timing

Asynchronous Mode Slave Read/Write Sequence:

1) R_W/, Address and the Size lines are asserted by the CPU.

2) Address Strobe is asserted by the CPU.

3) Chip Select is validated by the 53C710 on any following rising edge of BCLK.

4) Cache Burst Acknowledge is deasserted by the 53C710.

5) If a Write, the Data lines are asserted by the CPU.

5) Three clock cycles of wait state are inserted and, if a Read, the Data lines are asserted by the 53C710.

6) Slave Acknowledge is asserted by the 53C710 if the cycle ends normally or Bus Error is asserted if a bus error is detected.

7) Address Strobe is deasserted by the CPU.

8) Slave Acknowledge or Bus Error is deasserted by the 53C710 (and the data lines if a Read) are three-stated by the 53C710.

REF #	PARAMETER	MIN	MAX	UNIT
1	AS/ setup to CS/ clocked active	5	-	ns
2	A(5:0), SIZ(1:0), R-W/ setup to AS/	4	-	ns
3	A(5:0), SIZ(1:0), R-W/ hold from AS/	8	-	ns
4	CS/ setup to BCLK high after AS/	5	-	ns
5	CS/ hold from BCLK high after AS/	5	-	ns
6	BCLK high to SLACK/, BERR/ low	-	20	ns
7	AS/ high to SLACK/, BERR/ high	-	18	ns
8	STERM/ (Input) setup to BCLK high	2	-	ns
9	STERM/ (Input) hold From BCLK high	6	-	ns
10	BCLK high to Data Bus driven (Read Cycles)	8	-	ns
11	BCLK high to Read Data valid	-	65	ns
12	AS/ high to Data Bus Hi-Z	-	28	ns
13	Write Data setup to BCLK low	2	-	ns
14	Write Data hold from BCLK low	4	-	ns

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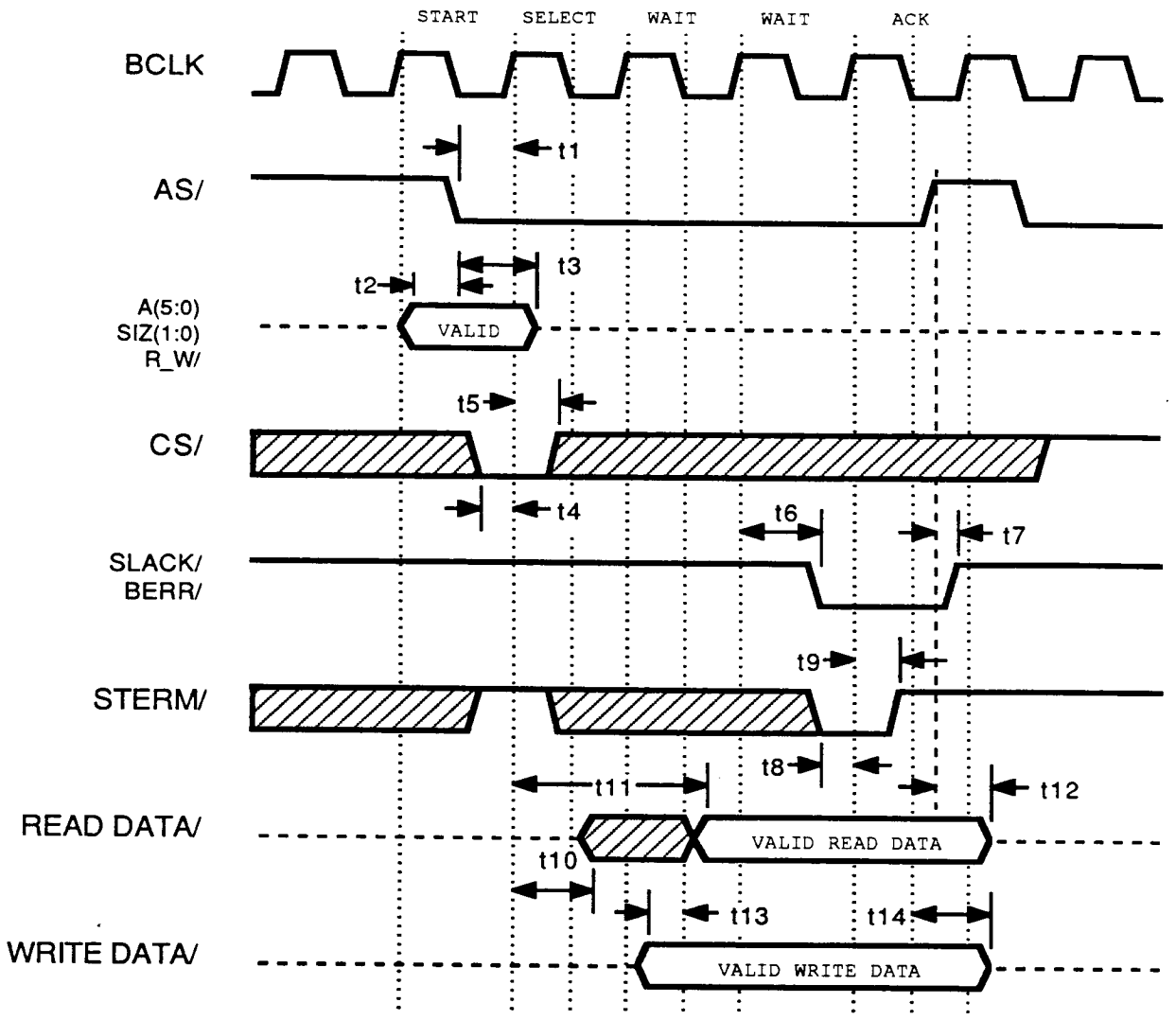
Asynchronous Mode Slave Read/Write



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Synchronous Slave Read/Write Timing

Synchronous Mode Slave Read/Write Sequence

1) R_W/, Address, Transfer Start and the Size lines are asserted by the CPU.

2) Chip Select is validated by the 53C710 on any following rising edge of BCLK.

3) Transfer Burst Inhibit is asserted.

4) Transfer Start is deasserted by the CPU.

5) If a Write, the Data lines are asserted by the CPU.

6) Three clock cycles of wait state are inserted and the Data lines are asserted (if a Read).

7) Slave Acknowledge is asserted by the 53C710, if no error.

8) If a bus error is detected, only Transfer Error Acknowledge is asserted and the bus cycle ends on the next rising edge of BCLK.

9) Slave Acknowledge or Transfer Error Acknowledge is deasserted.

10) The 53C710 waits for Transfer Acknowledge to be asserted and then ends the slave cycle, id no error.

11) If a Read, the data lines are three-stated by the 53C710.

REF #	PARAMETER	MIN	MAX	UNIT
1	TS/ setup to BCLK high	4	-	ns
2	TS/ hold from BCLK high	4	-	ns
3	CS/ setup to BCLK high after TS/	5	-	ns
4	CS/ hold from BCLK high after TS/	5	-	ns
5	BCLK high to SLACK/, TEA/ low	-	18	ns
6	BCLK high to SLACK/, TEA/ high	-	16	ns
7	TA/ setup to BCLK high during or after SLACK/, TEA/	9	-	ns
8	TA/ hold from BCLK high during or after SLACK/, TEA/	2	-	ns
9	BCLK high to Data Bus driven (Read Cycles)	8	-	ns
10	BCLK high to Read Data valid	-	65	ns
11	BCLK high to Data Bus Hi-Z	-	34	ns
12	Valid Write Data setup to BCLK high	5	-	ns
13	Valid Write Data hold from BCLK high	6		ns
14	A(5:0), SIZ(1:0), R-W/ setup to BCLK high	2	-	ns
15	A(5:0), SIZ(1:0), R-W/ hold from BCLK high	12	-	ns

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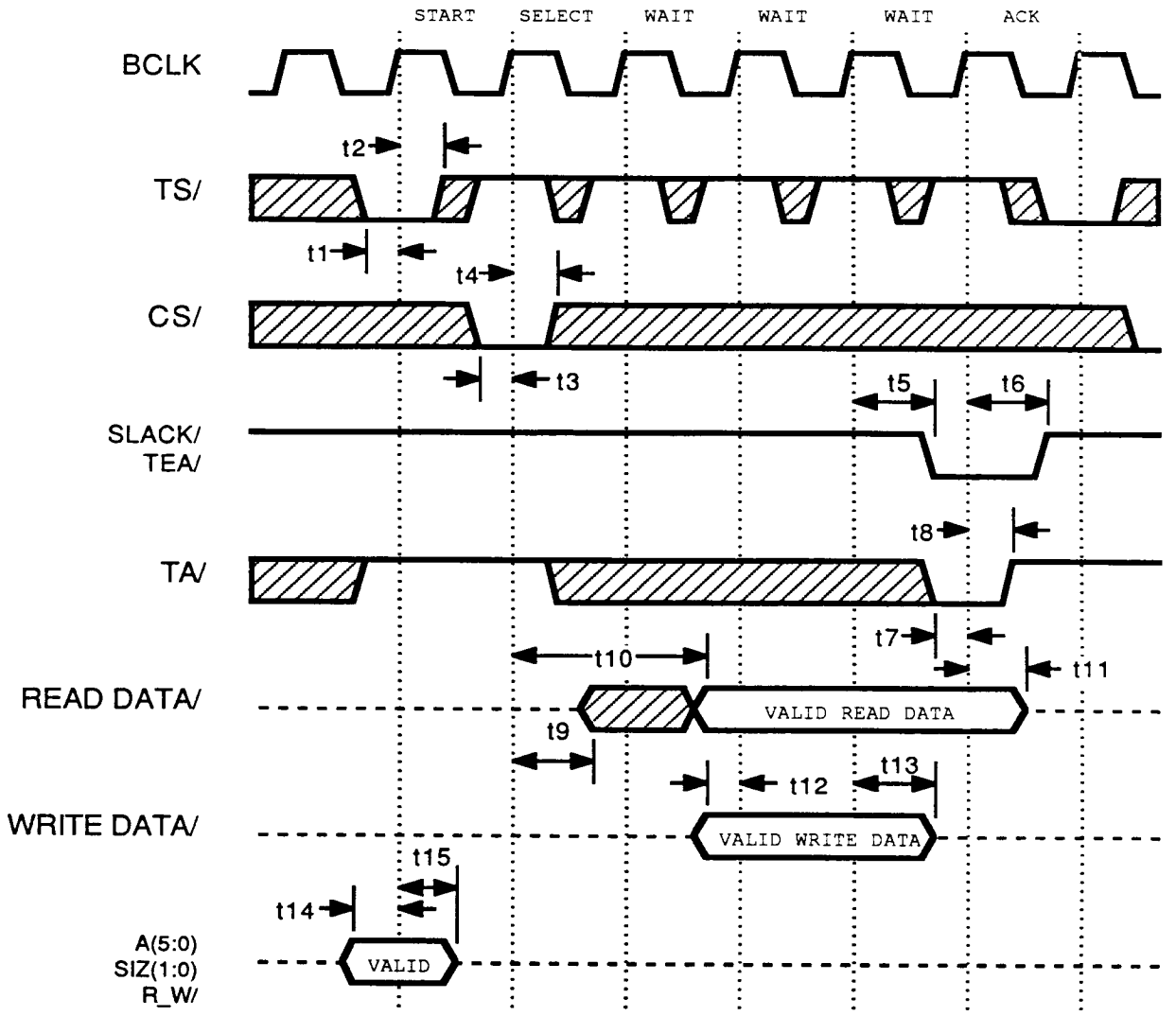
Synchronous Mode Slave Read/Write



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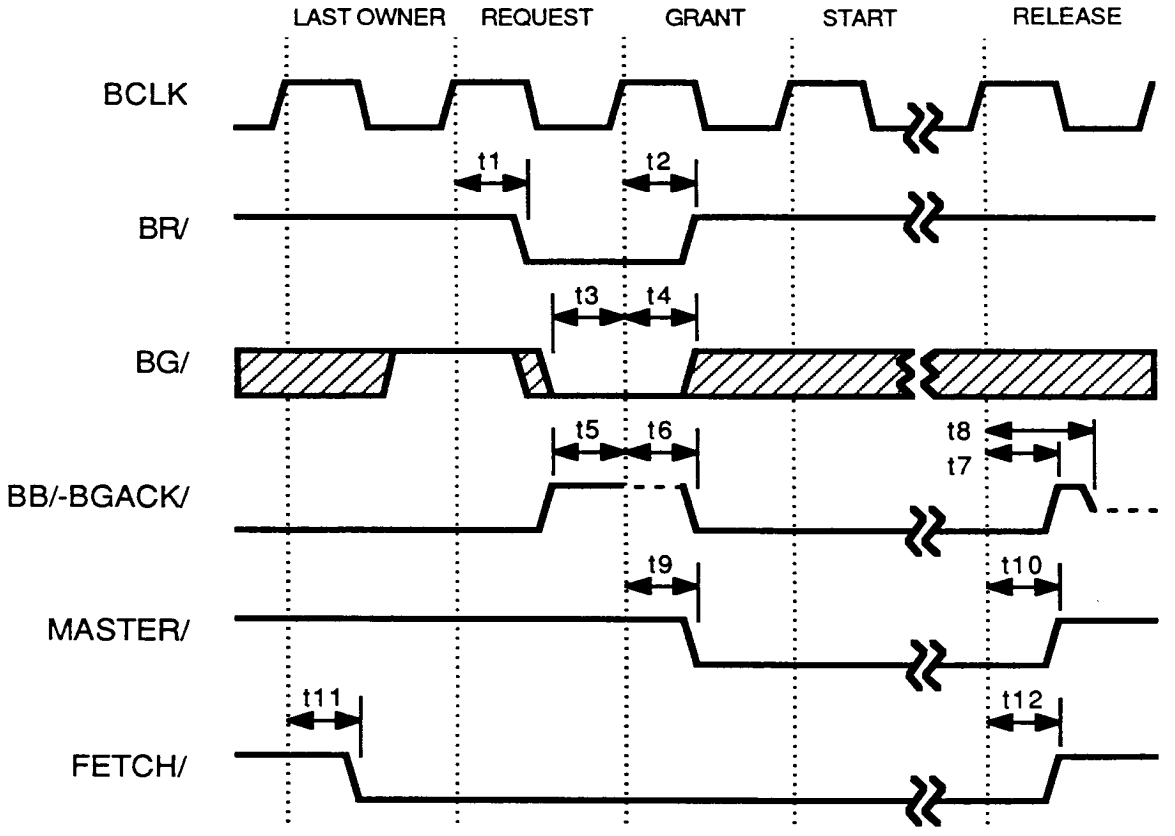
Host Bus Arbitration

Bus Arbitration Sequence

1) The 53C710 internally determines bus mastership is required. If appropriate, FETCH/ is asserted.

2) Bus Request is asserted.

3) The 53C710 waits for Bus Grant and checks that Bus Grant Acknowledge is deasserted. Then the 53C710 asserts Bus Grant Acknowledge and Master, and deasserts Bus Request.



REF #	PARAMETER	MIN	MAX	UNIT
1	BCLK high to BR/ low	-	17	ns
2	BCLK high to BR/ high	-	22	ns
3	BG/ setup to BCLK high (any rising edge after BR/)	4	-	ns
4	BG/ hold from BCLK high (any rising edge after BR/)	5	-	ns
5	BB/-BGACK/ setup to BCLK high (any rising edge after BR/)	5	-	ns
6	BCLK high to BB/-BGACK/ low	-	24	ns
7	BCLK high to BB/-BGACK/ high	-	13	ns
8	BCLK high to BB/-BGACK/ high-Z	-	32	ns
9	BCLK high to MASTER/ low	-	18	ns
10	BCLK high to MASTER/ high	-	21	ns
11	BCLK high to FETCH/ low	-	26	ns
12	BCLK high to FETCH/ high	-	28	ns

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Asynchronous Bus Master Timings

Asynchronous Mode Bus Master Read/Write Sequence

1) The 53C710 has attained bus mastership.

2) The 53C710 asserts the R_W/, Snoop Control, Function Control and Transfer Type lines.

3) The 53C710 asserts the Address and Size lines (and Data lines if Write).

4) The 53C710 asserts Address Strobe and Cache Burst Request (and Data Strobe if Read).

5) If a Write, the 53C710 asserts Data Strobe.

5) The 53C710 waits for Synchronous Termination, valid data (if Read), Cache Burst Acknowledge, Bus Error and HALT.

   • If Cache Burst Acknowledge is asserted, attempt bursting.

   • If Bus Error and Halt are asserted, attempt a retry.

   • If synchronous termination is asserted without Bus Error or HALT, and the 53C710 requires more cycles, then return to function 3.

6) The 53C710 deasserts the control and Address lines (and Data lines if Write).

7) Upon Acknowledge of the last bus cycle, the 53C710 deasserts Master and Bus Grant Acknowledge.

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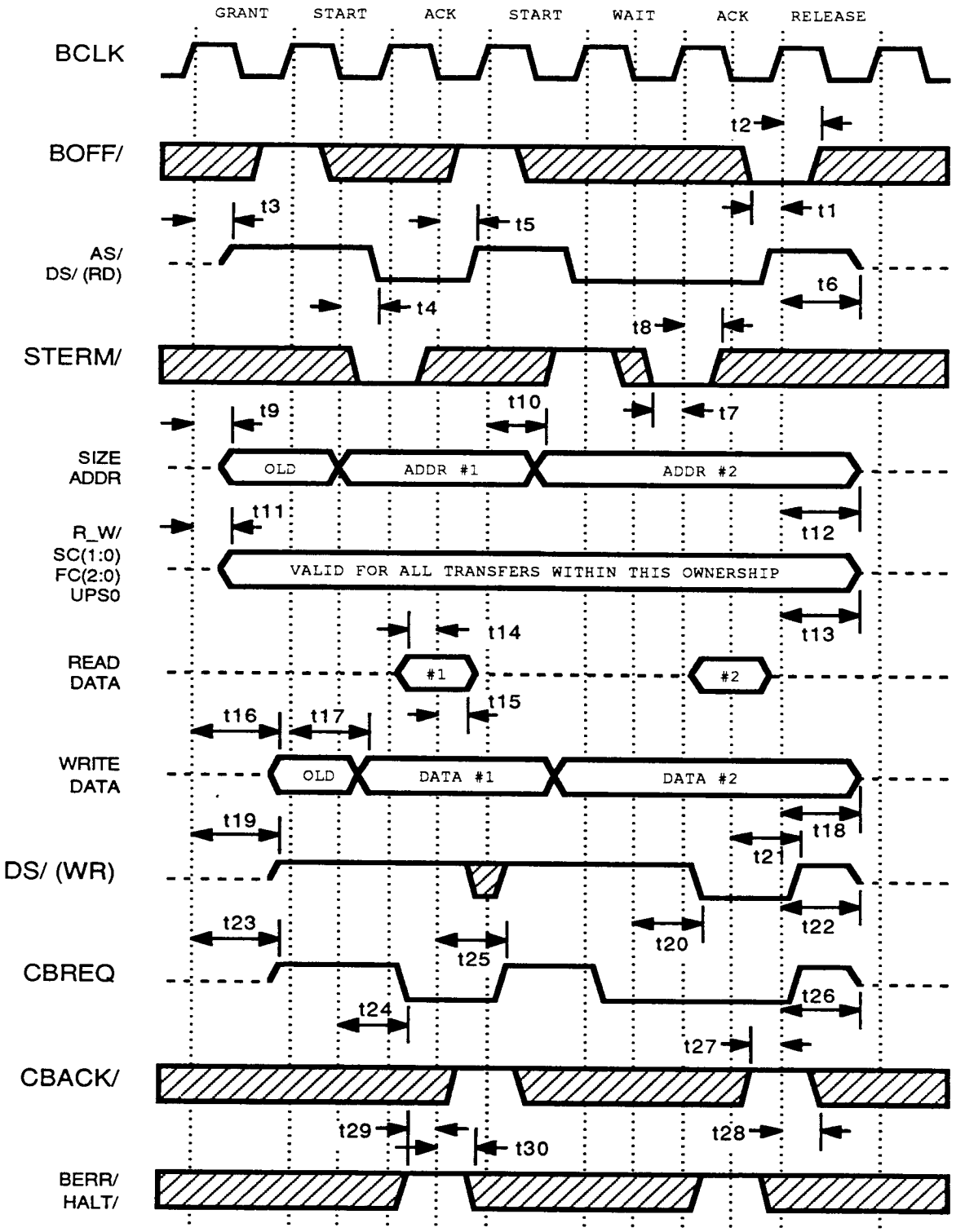
Asynchronous Mode Bus Master, Non-Cache-Line Burst



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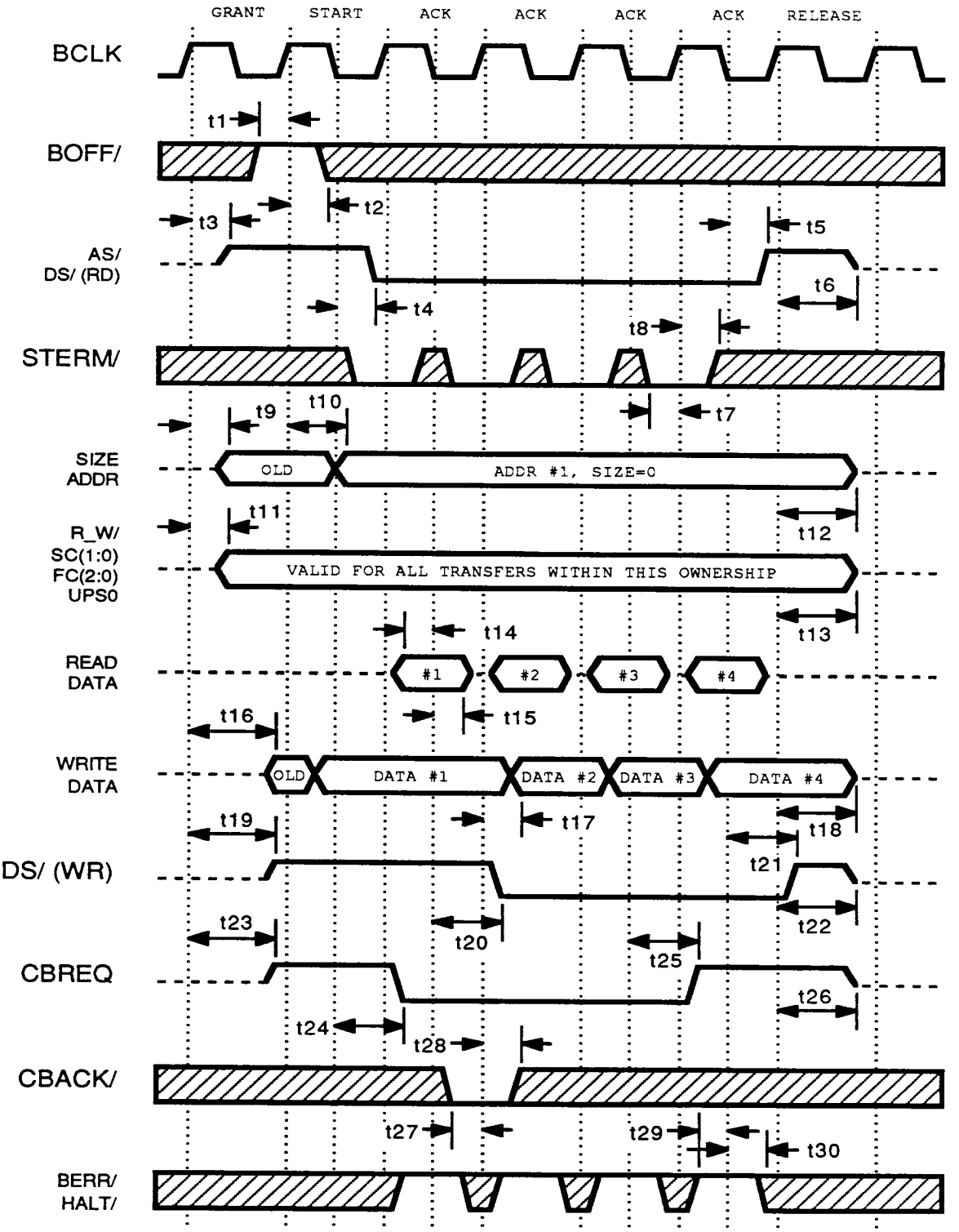
Asynchronous Mode Bus Master, Cache-Line Burst



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Asynchronous Mode Bus Master, Non-Cache-Line & Cache-Line Burst

REF #	PARAMETER	MIN	MAX	UNIT
1	BOFF/ setup to BCLK high	4	-	ns
2	BOFF/ hold from BCLK high	6	-	ns
3	BCLK high to AS/, DS/ driven	-	32	ns
4	BCLK low to AS/ (and DS/) low	-	14	ns
5	BCLK low to AS/ (and DS/) high	-	14	ns
6	BCLK high to AS/, DS/ Hi-Z	-	34	ns
7	STERM/ (Input) setup to BCLK high	3	-	ns
8	STERM/ (Input) hold from BCLK high	7	-	ns
9	BCLK high to Size, Address driven	-	28	ns
10	BCLK high to Size, Address valid	-	17	ns
11	BCLK high to R-W/, SC(1:0), FC(2:0), UPSO driven and valid	-	28	ns
12	BCLK high to Size, Address Hi-Z	-	34	ns
13	BCLK high to R-W/, SC(1:0), FC(2:0), UPSO Hi-Z	-	30	ns
14	Read Data setup to BCLK low	2	-	ns
15	Read Data hold from BCLK low	4	-	ns
16	BCLK high to Write Data driven	-	34	ns
17	BCLK high to Write Data valid	-	24	ns
18	BCLK high to Data Hi-Z	-	32	ns
19	BCLK high to DS/ (write) driven	-	32	ns
20	BCLK low to DS/ (write) low	-	14	ns
21	BCLK low to DS/ (write) high	-	14	ns
22	BCLK high to DS/ (write) Hi-Z	-	34	ns
23	BCLK high to CBREQ/ driven	-	30	ns
24	BCLK low to CBREQ/ low	-	16	ns
25	BCLK low to CBREQ/ high	-	14	ns
26	BCLK high to CBREQ/ Hi-Z	-	32	ns
27	CBACK/ setup to BCLK high	6	-	ns
28	CBACK/ hold from BCLK high	4	-	ns
29	BERR/, HALT/ setup to BCLK low	6	-	ns
30	BERR/, HALT hold from BCLK low	4	-	ns

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Synchronous Bus Master Timings

Synchronous Mode Bus Master Read/Write Sequence

1) The 53C710 has attained bus mastership.

2) The 53C710 asserts the R_W/, Snoop Control, Function Control and Transfer Type lines.

3a) The 53C710 asserts Transfer In Progress and Transfer Start.

3b) The 53C710 asserts Transfer Start, Address, and Size lines (and Data lines if Write).

4) The 53C710 deasserts Transfer Start.

5) The 53C710 waits for Transfer Acknowledge, valid data (if Read), Transfer Burst Inhibit and Transfer Error Acknowledge.

   • If Transfer Burst Inhibit is not asserted, attempt cache bursting.

   • If Transfer Error Acknowledge and Transfer Acknowledge are asserted, attempt a retry.

   • If Transfer Error Acknowledge is asserted and Transfer Acknowledge is not asserted, a bus fault condition will be generated.

   • If Transfer Acknowledge is asserted and Transfer Error Acknowledge is not asserted and the 53C710 requires more cycles, then return to 3b.

6) The 53C710 deasserts the control, Address and Data lines (if Write).

7) Upon Acknowledge of the last bus cycle, the 53C710 deasserts Master and Bus Grant Acknowledge.

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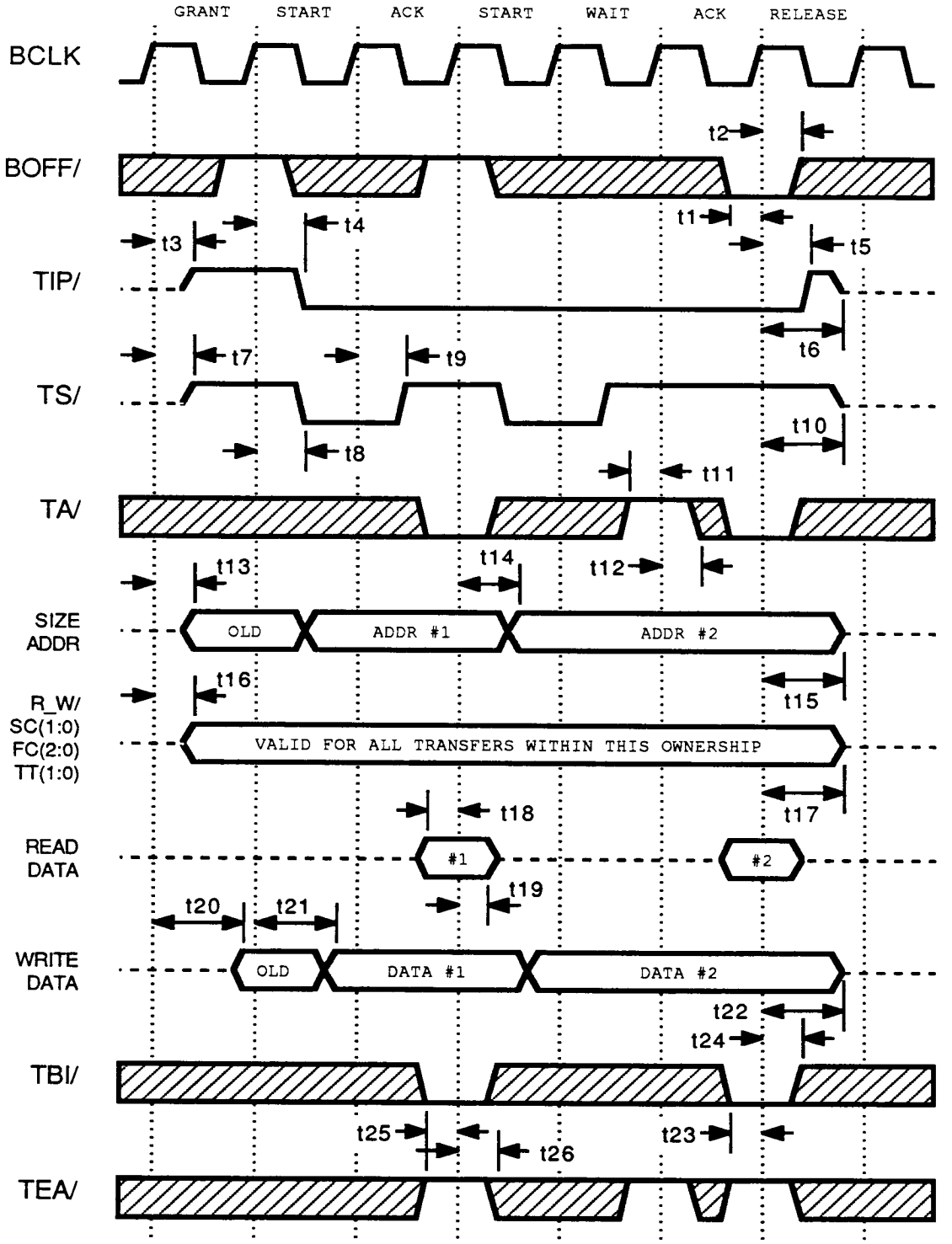
Synchronous Mode Bus Master, Non-Cache-Line Burst



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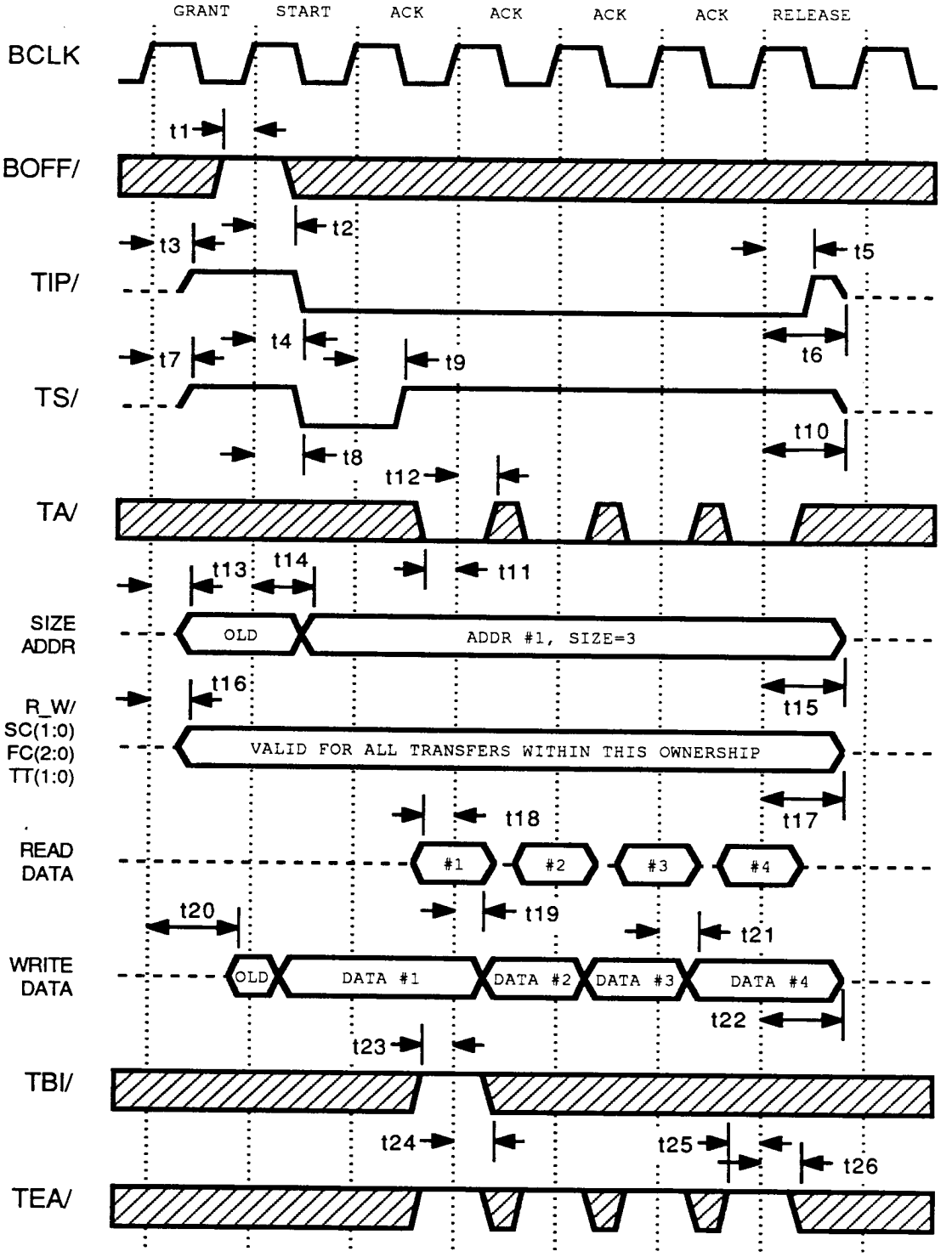
Synchronous Mode Bus Master, Cache-Line Burst



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Synchronous Mode Bus Master, Non-Cache-Line & Cache-Line Burst

REF #	PARAMETER	MIN	MAX	UNIT
1	BOFF/ setup to BCLK high	4	-	ns
2	BOFF/ hold from BCLK high	6	-	ns
3	BCLK high to TIP/ driven	-	32	ns
4	BCLK high to TIP/ low	-	15	ns
5	BCLK high to TIP/ high	-	14	ns
6	BCLK high to TIP/ Hi-Z	-	32	ns
7	BCLK high to TS/ driven	-	30	ns
8	BCLK high to TS/ low	-	14	ns
9	BCLK high to TS/ high	-	13	ns
10	BCLK high to TS/ Hi-Z	-	32	ns
11	TA/ setup to BCLK high	9	-	ns
12	TA/ hold from BCLK high	5	-	ns
13	BCLK high to A(31:0), SIZ(1:0) driven	-	28	ns
14	BCLK high to A(31:0), SIZ(1:0) valid	-	18	ns
15	BCLK high to A(31:0), SIZ(1:0) Hi-Z	-	32	ns
16	BCLK high to R-W/, SC(1:0), FC(2:0), TT(1:0) driven and valid	-	30	ns
17	BCLK high to R-W/, SC(1:0), FC(2:0), TT(1:0) Hi-Z	-	32	ns
18	Read Data setup to BCLK high	4	-	ns
19	Read Data hold from BCLK high	6	-	ns
20	BCLK high to Write Data driven	-	34	ns
21	BCLK high to Write Data valid	-	24	ns
22	BCLK high to Write Data Hi-Z	-	28	ns
23	TBI setup to BCLK high	6	-	ns
24	TBI hold from BCLK high	4	-	ns
25	TEA setup to BCLK high	6	-	ns
26	TEA hold from BCLK high	4	-	ns

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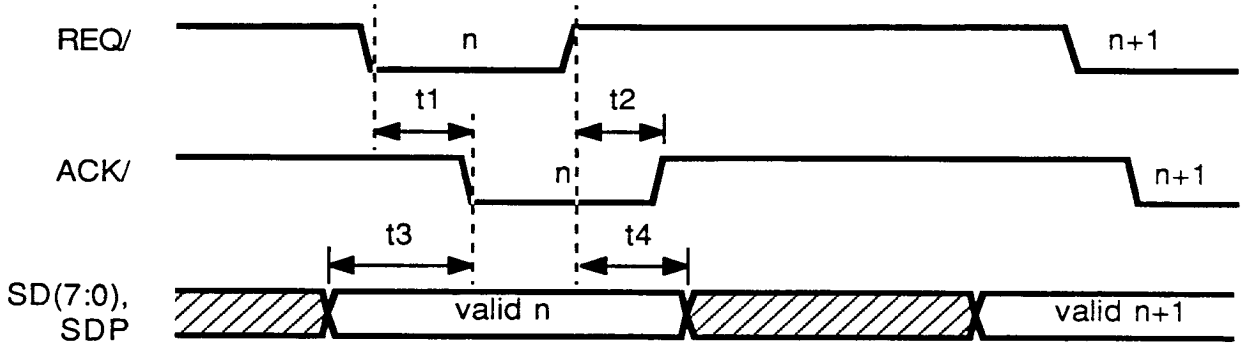
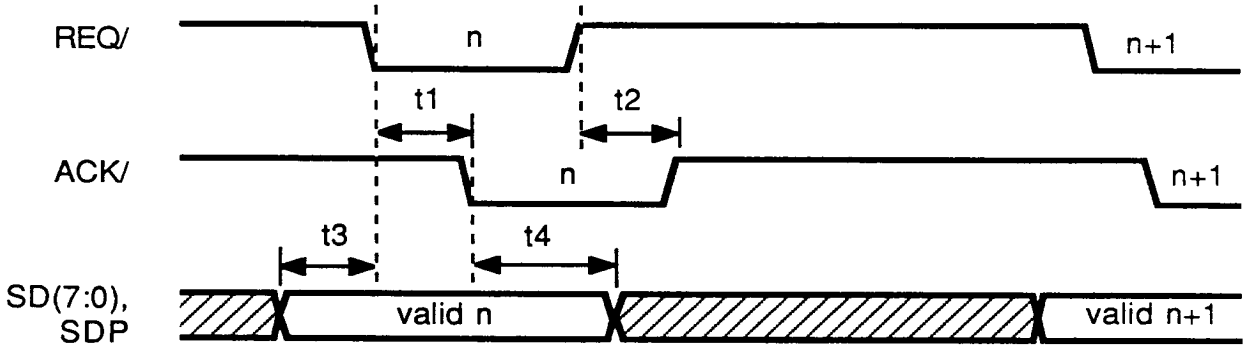
Initiator Asynchronous Send



REF #	PARAMETER	MIN	MAX	UNIT
1	ACK/ asserted from REQ/ asserted	10	-	ns
2	ACK/ deasserted from REQ/ deasserted	10	-	ns
3	Data setup to ACK/ asserted	55	-	ns
4	Data hold from REQ/ deasserted	20	-	ns

Initiator Asynchronous Receive



REF #	PARAMETER	MIN	MAX	UNIT
1	ACK/ asserted from REQ/ asserted	10	-	ns
2	ACK/ deasserted from REQ/ deasserted	10	-	ns
3	Data setup to REQ/ asserted	0	-	ns
4	Data hold from ACK/ deasserted	0	-	ns

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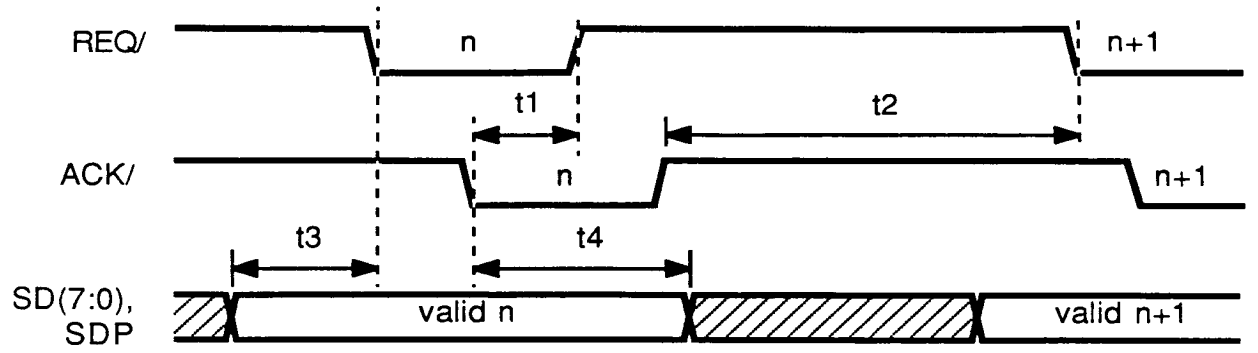
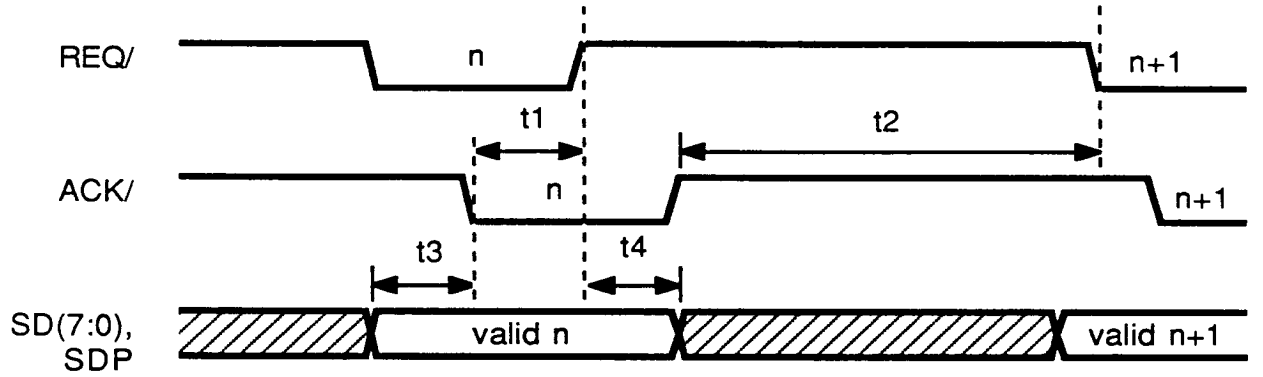
Target Asynchronous Send



REF #	PARAMETER	MIN	MAX	UNIT
1	REQ/ deasserted from ACK/ asserted	10	-	ns
2	REQ/ asserted from ACK/ deasserted	10	-	ns
3	Data setup to REQ/ asserted	55	-	ns
4	Data hold from ACK/ asserted	20	-	ns

Target Asynchronous Receive



REF #	PARAMETER	MIN	MAX	UNIT
1	REQ/ deasserted from ACK/ asserted	10	-	ns
2	REQ/ asserted from ACK/ deasserted	10	-	ns
3	Data setup to ACK/ asserted	0	-	ns
4	Data hold from REQ/ deasserted	0	-	ns

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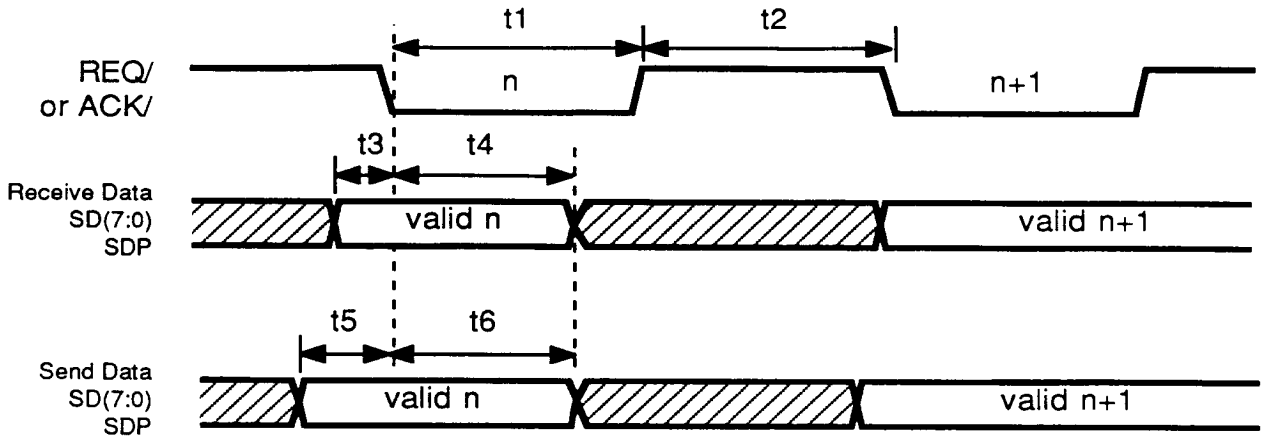
Initiator and Target Synchronous Transfers



SCSI-1 Transfers

REF #	PARAMETER	MIN	MAX	UNIT
1	REQ/ or ACK/ assertion pulse width	90	-	ns
2	REQ/ or ACK/ deassertion pulse width	90	-	ns
3	Receive data setup to REQ/ or ACK/ asserted	0	-	ns
4	Receive data hold from REQ/ or ACK/ asserted	45	-	ns
5	Send data setup to REQ/ or ACK/ asserted	55	-	ns
6	Send data hold from REQ/ or ACK/ asserted	100	-	ns

SCSI-2 Fast Transfers

REF #	PARAMETER	MIN	MAX	UNIT
1	REQ/ or ACK/ assertion pulse width	40	-	ns
2	REQ/ or ACK/ deassertion pulse width	40	-	ns
3	Receive data setup to REQ/ or ACK/ asserted	0	-	ns
4	Receive data hold from REQ/ or ACK/ asserted	10	-	ns
5	Send data setup to REQ/ or ACK/ asserted	40	-	ns
6	Send data hold from REQ/ or ACK/ asserted	35	-	ns

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Appendix A - 53C710 Feature/Benefit Summary

Benefit	Feature
PERFORMANCE	- Supports Variable block Size and scatter/gather data transfers
	- Supports 32-bit word data bursts with variable burst lengths
	- Memory-to-Memory DMA transfers
	- Minimizes SCSI I/O start latency
	- Performs complex bus sequences without interrupts including Restore Data Pointers
	- Unique interrupt status reporting - reduces ISR overhead
	- High-speed async/sync SCSI Bus Transfers Over 5 MBytes/sec asynchronous 10 MBytes/sec synchronous
	- Memory transfers in excess of 66 MBytes/sec (@ 33 MHz)
	- Cache-Line Burst Mode.
	- 64-byte DMA FIFO
INTEGRATION	- Full 32-bit DMA bus master
	- High performance SCSI Core
	- Integrated SCRIPTs PROCESSOR
	- Allows intelligent host adapter performance on a motherboard
FLEXIBILITY	- High-level programmer's interface (SCSI SCRIPTs)
	- Allows tailored SCSI sequences to be executed from main memory or from a host adapter board.
	- Flexible sequences to tune I/O performance or to adapt to unique SCSI devices
	- Accommodates changes in the logical I/O interface definition
	- Low level programmability (register oriented)
	- Allows a target to disconnect and later be reselected with no interrupt to the system processor
	- Allows a multi-threaded I/O algorithm to be executed in SCSI SCRIPTs with a fast I/O context switch.
	- Can auto-switch between initiator and target roles dynamically
	- Allows relative jumps

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- Allows indirect fetching of DMA address and byte counts so that SCRIPTs can be placed in a PROM.
- Separate SCSI and system clocks

EASE OF USE

- Reduces SCSI development effort
- Emulates existing intelligent host adapters
- Support for big and little Endian environments.
- Easily adapted to the SCSI Common Access Method (CAM) by "executing" data structures
- Fully compatible with existing 53C700 SCRIPTs
- Development tools and SCSI SCRIPTs provided
- All interrupts are maskable and pollable

RELIABILITY

- 10K Volts ESD protection SCSI Signals
- Typical 350 mV SCSI Bus Hysteresis
- Protection against Bus Reflections due to Impedance Mismatches
- Controlled Bus Assertion Times (reduces RFI, improves reliability, and eases FCC certification)
- Latch-up protection greater than 100 mA
- 250 milliseconds byte-to-byte SCSI activity timer
- Voltage feed through protection (minimum leakage current through SCSI pads)
- 20% of signals are power and ground
- Ground isolation of I/O pads and chip logic

TESTABILITY

- All SCSI signals accessible through programmed I/O
- SCSI Loopback Diagnostics
- Self-selection capability
- SCSI bus signal continuity checking

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Appendix B - Migrating 53C700 Software

The 53C710 can execute all 53C700 SCRIPTs without recompilation. However, because there are new registers and bits, and some registers and bits have been relocated or deleted, firmware drivers will need to be modified. The table below summarizes the differences between the 53C700 and 53C710 register sets.

NEW

ITEM	53C700	53C710
Synchronous SCSI Clock Control Bits	n/a	SBCL, bits 1-0
Bus Fault Bit	n/a	DSTAT, bit 5
Data Structure Address Register	n/a	DSA
SIGnal Process Test & Reset Bit	n/a	CTEST2, bit 6
MUX Mode Bit	n/a	CTEST4, bit 7
Cache Burst Disable Bit	n/a	CTEST7, bit 7
Snoop Control Bits 1-0	n/a	CTEST7, bits 6-5
Transfer Type One Bit	n/a	CTEST7, bit 1
Byte Offset Six Bit	n/a	DFIFO, bit 6
SIGnal Process Set Bit	n/a	ISTAT, bit 5
FETCH/ Pin Control Bit	n/a	CTEST8, bit 1
Snoop Mode Bit	n/a	CTEST8, bit 0
LCRC Register	n/a	LCRC
Scratch Register	n/a	SCRATCH
Function Code Bits 2-1	n/a	DMODE, bits 5-4
Program/Data Function Code 0 Control Bit	n/a	DMODE, bit 3
UPSO-TT0/ Bit	n/a	DMODE, bit 1
Bus Fault Interrupt Enable Bit	n/a	DIEN, bit 5
Enable Acknowledge Control Bit	n/a	DCNTL, bit 5
Fast Arbitration Mode Bit	n/a	DCNTL, bit 1
53C700 Compatibility Bit	n/a	DCNTL, bit 0
Adder Output Register	n/a	ADDER

DELETED

ITEM	53C700	53C710
DC/ Pin Control Bit	CTEST7, bit 1	n/a
DSPS and DSP Empty Bit	ISTAT, bit 2	n/a
16-Bit DMA, '286-Mode Bits	DMODE, bits 5-4	n/a
I/O-Memory Mapped DMA Bit	DMODE, bit 3	n/a
Pipeline Mode Bit	DMODE, bit 1	n/a
16-Bit SCSI Scripts Mode Bit	DCNTL, bit 5	n/a
Real Target Mode Bit	CTEST0, bit 1	n/a

MOVED

ITEM	53C700	53C710
Flush FIFO Bit	DFIFO, bit 7	CTEST8, bit 3
Clear FIFO Bit	DFIFO, bit 6	CTEST8, bit 2
Software Reset Bit	DCNTL, bit 0	ISTAT, bit 6
Chip Revision Level Bits	CTEST7, bits 7-4	CTEST8, bits 7-4
DMODE Register	Address 34h	Address 38h

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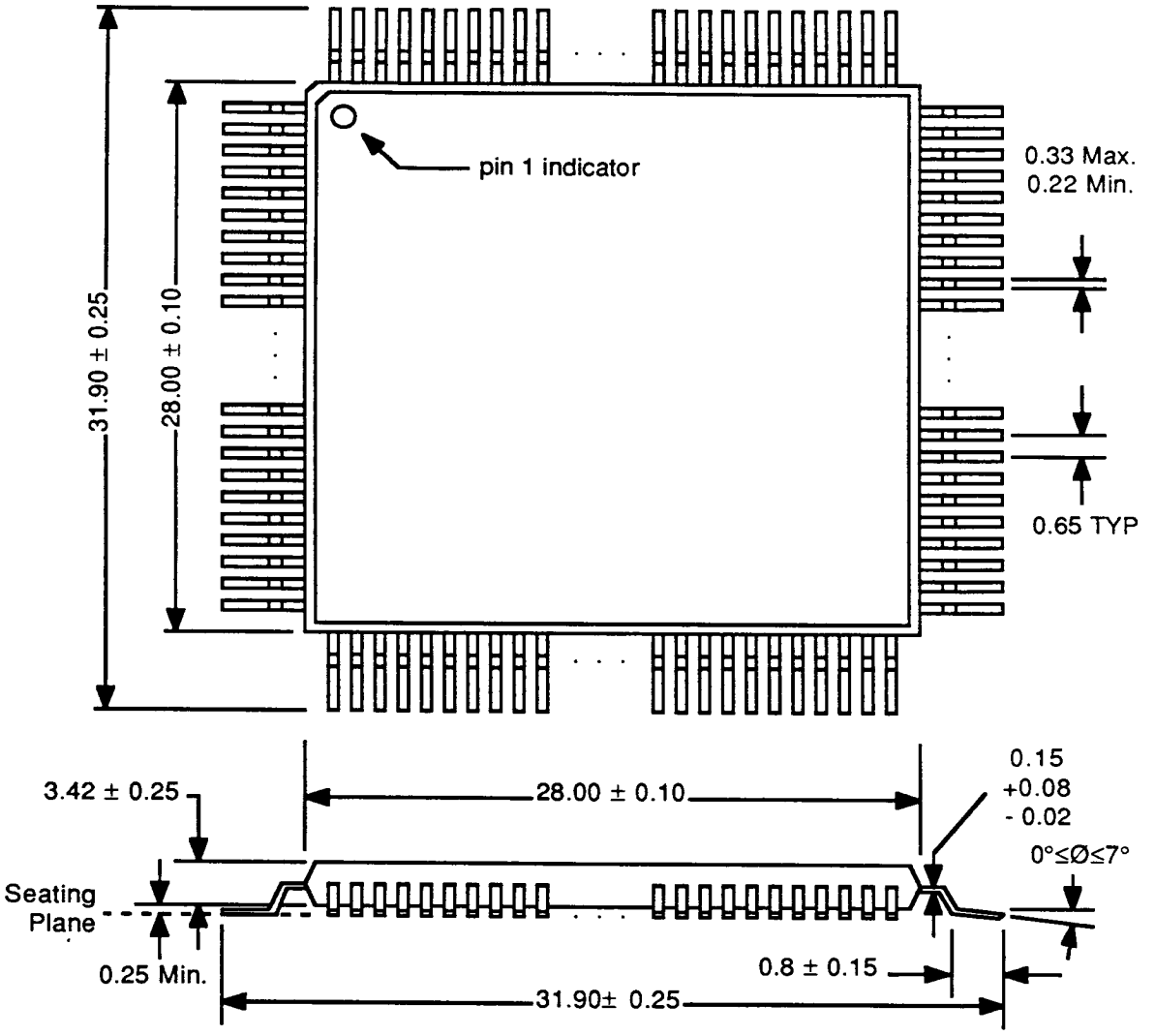
Appendix C - 160 QFP Mechanical Drawing



Note: All dimensions are in millimeters. This package is known as a Metric QFP, and should not be confused with the similar JEDEC QFP.

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