SCHEMATICS
AND
EXPANSION
SPECIFICATIONS

June 9, 1986

PAL EQUATIONS

PAL16L8
DPALCAS 252128-02 REV 3
15-MAY-85

/ARW A20 A19 /PRW /UDS /LDS /ROME /RE /RGAE GND /DAE /ROM01
/C1 /RRW LCEN UCEN /CDR /CDW /NC1 VCC

```
ROMO1    =ROME*A20*A19*/PWR + ROME*/A20*/A19*/PRW
CDR      =RE*/PWR*/C1 +  RGAE*/PRW*/C1 + CDR*LDS + CDR*UDS
CDW      =RE*PRW + RGAE*PRW + CDW*/C1 + /DAE*/UDS*/UCEN
/UCEN    =/DAE*/RE*/UCEN + /DAE*/RE*C1 +/DAE*UDS*C1 + /DAE*/UDS*/UCEN
/LCEN    =/DAE*/RE*/LCEN + /DAE*/RE*C1 +/DAE*/LDS*C1 + /DAE*/LDS*/LCEN
RRW      =RE*PRW + DAE*ARW*C1 + RRW*DAE
```

Description

In RRW equation, may not need RRW*/C1 hold term, but doesn't hurt

PRELIMINARY

PAL 16L8
DAUGCAS ram/rom CAS 252128-04 REV 1
16-APR-85

/SPROM A18 A17 /PRW /UDS /LDS /RE /RES /ROME GND /C1 /BERR
/WPRO /RRW /LCEN /UCEN /CDR /CDW /ROMO1 VCC

```
ROMO1   =ROME*/A18*/WPRO*/SROM*/PRW
CDR     =CDR*LDS + CDR*UDS + RE*/PRW*/C1*A18 + RE*/PRW*/C1*/A18*WPRO
         + RE*/PRW*/C1/A18*SROM
CDW     = RE*PRW + CDW*/C1
UCEN    =UCEN*/C1 + RE*UDS*A18  RE*UDS*/A18*WPRO +
         RE*UDS*/A18*SROM
LCEN    =LCEN*/C1 + RE*LDS*A18 + RE*LDS*/A18*WPRO +
          RE*LDS*/A18*SROM
RRW     =RE*PRW*A18/WPRO*/SROM
BERR    =WPRO*PRW*RE
WPRO    =WPRO*/RES + PRW*RE/A18
```

Description

This is the CAS PAL for the RAMROM board

PRELIMINARY

PORT DESCRIPTORS

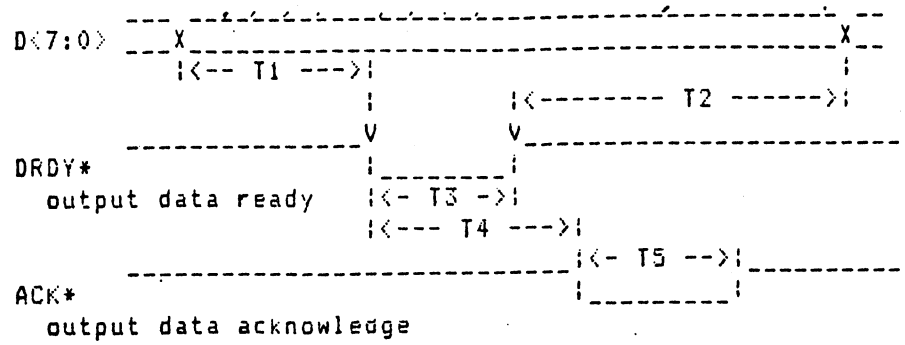
Parallel Interface Connector Specification

The 25 pin D type connector with pins (DB25P) at the rear of the Amiga is nominally used to interface to parallel printers. In this capacity, data flows from the Amiga to the printer. This interface may also be used for input or bidirectional data transfers. The implementation is similar to Centronics, but the pin assignment and drive characteristics vary significantly from the specification.

Parallel Connector Pin Assignment (J8)

Pin	Name	dir	Notes
1	DRDY*	O	Output data ready signal to parallel devices in output mode, used in conjunction with ACK* (pin 10) for a 2 line asynchronous handshake. Functions as input data accepted from Amiga in input mode (similar to ACK* in output mode). See timing diagrams in following section.
2	DO	I/O	
3	D1	I/O	
4	D2	I/O	
5	D3	I/O	D0–D7 comprise an 8 bit bidirections bus for communication with parallel devices, nominally, a printer.
6	D4	I/O	
7	D5	I/O	
8	D6	I/O	
9	D7	I/O	
10	ACK*	I	Output data acknowledge from parallel device in output mode, used in conjunction with DRDY* (pin 1) for a 2 line asynchronous handshake. Functions as input data ready from parallel device in input mode (similar to DRDY* in output mode). See timing diagram in following section. The 8520 can be programmed to conditionally generate a level 2 interrupt to the 68000 whenever the ACK* input goes active.
11	BUSY	I/O	This is a general purpose I/O pin shorted to a serial data I/O pin (serial clock on pin 12). Note: Nominally used to indicate printer buffer full.
12	POUT	I/O	This is a general purpose I/O pin shored to a serial clock I/O pin (serial data on pin 11). Note: Nominally used to indicate printer paper out.

Parallel Connector Interface Timing, Output Cycle



	microseconds min	typ	max	
T1:	4.3		5.3	Output Data setup to ready delay
T2:	nsp		upc	Output Data hold time.
T3:	nsp	1.4	nsp	Output Data ready width
T4:	0		upc	Ready to acknowledge delay
T5:	nsp		upc	Acknowledge width

nsp = not specified
upc = under program control

PRELIMINARY

Serial Interface Connector Specification

The 25 pin D type connector with sockets (DB25S) is used to interface to RS232C standard signals.

WARNING: Pins 14, 21 and 23 carry power. Do not connect to these pins inadvertantly as they can permanently damage external equipment. Also, pins 15–18, 23–25 carry non–standard signals and should not be inadvertantly connected.

NEVER use a fully wired 25 line cable!

Serial Interface Connector Pin Assignment (J6)

Pin	Name	Dir	Std	Notes
1	FGND		y	frame ground
2	TXD	0	y	transmit data
3	RXD	I	y	receive data
4	RTS	0	y	request to send
5	CTS	I	y	clear to send
6	DSR	I	y	data set ready
7	GND		y	signal ground
8	CD	I	y	carrier detect
9	---		n	
10	---		n	
11	---		y	
12	---		n	
13	---		n	
14	-5V		n*	50 ma maximum
15	AUDO	0	n*	audio output
16	AUDI	I	n*	audio input
17	EB	0	n*	716 KHz
18	INT2*	I	y	OPEN COLLECTOR Amiga Interrupt level 2
19	---		n	
20	DTR	0	y	data terminal ready
21	+5V		n*	100 ma maximum
22	---		n	
23	+12V		n*	50 ma maximum
24	C2*	0	n*	3.58 MHz
25	RESB*	0	n*	Amiga system reset

n*:
WARNING: Pins 14, 21 and 23 carry power. Do not connect to these pins inadvertantly as they can permanently damage external equipment. Also, pins 15–18, 23–25 carry non–standard signals and should not be inadvertantly connected.
NEVER use a fully wired 25 line cable!

External Disk Interface Connector Specification

The 23 pins D type connector with sockets (DB23S) at the rear of the Amiga is nominally used to interface to MFM devices.

External Disk Connector Pin Assignment (J7)

Pin	Name	Dir	Notes
1	RDY*	I/O	If motor on, indicates disk installed and up to speed If motor not on, Identification mode. See below.
2	DKRD*	I	MFM input data to Amiga
3	GND		
4	GND		
5	GND		
6	GND		
7	GND		
8	MTRXD*	OC	Motor on data, clocked into drive's motor on flip flops by the active transistion of SELxB*. Guaranteed setup time is 1.4 usec. Guaranteed hold time is 1.4 used.
9	SEL2B*	OC	Select drive 2
10	DRESB*	OC	Amiga system reset. Drive should reset their motor on flip flops and set their write protect flip flops.
11	CHNG*	I/O	Note: Nomially used as an open collector input. Drives change flop is set at powe up or when no disk is not installed. Flop is reset when drive is selected and the head stepped, but only is a disk is installed.
12	+5V		270 ma maximum; 410 ma surge When below 3.75V, drives are required to reset their motor on flops, and set their write protect on flops.
13	SIDEB*	O	Side 1 if active, side 0 if inactive
14	WPRO*	I/O	Asserted by selected, write protected disk
15	TKO*	I/O	Asserted by selected drive when read/write head is positioned over track 0
16	DKWDB*	OC	Write gate (enable) to drive
17	DKWDB*	OC	MFM output data from Amiga
18	STEPB*	OC	Selected drive steps one cylinder in the direction indicated by DIRB.
19	DIRB	OC	Direction to step the head. Inactive to step towards center of disk (higher humbered tracks).
20	SEL3B*	OC	Select drive 3
21	SEL1B	OC	Select drive 1
22	INDEX*	I/O	Index is a pulse generated once per disk revolution, between the end and geginning of cyliners. The 8520 can be programmed to conditinally generate a level 6 interrupt to the 68000 whenever the INDEX* input goes active
23	+12V		160 ma maximum; 540 ma surge

********** MEMO **********

Commodore-Amiga

TO: Hardware Developers
FM: H. Stolz - C=AMIGA
DT: 4/17/86

Dear developer;

In this package are the latest drawings of the Expansion Boards for the Amiga. We are releasing these drawings to you with the warning that the dimensions may change and are not final until FCC testing is completed. We feel confident about the 24.0mm (.945 in) center to center on the PCB's and we hope to increase the maximum component height allowed if the current rear panel scheme works out.

The Zorro Backplane Bd. Control Drawing # 327310-01 is included for refrence only. It is a board that was intended for lab use only and is not indicative of the Production backplane PCB.

PRELIMINARY

4-24-86

Dear Hardware Developers,

This memo is to inform you of two updates to the expansion architecture.

The first is that Amiga will put -12Volts @ 250ma on pin 20 of the hundred pin connector. This voltage is optional on 3rd party expansion boxes. Boards should be designed to not use this current, because Amiga has aleady assigned it's use. We recommend that you do include this voltage unless the cost is prohibitive (for instance if you have already ordered power supplies that do not include -12V.)

The other addition is that the RES* line needs a 10K pullup resistor. You must not put more than one load on RES*, and you should make this load as small as possible.

I apologize that these minor additions keep trickling in. However, we are developing this standard as fast as we can, and are trying to give you third party developers the earliest possible notice of our work. At this time, the changes are all minor and only those that are absolutely necessary are made.

Amiga Engineering

Designing Hardware for the Amiga Expansion Architecture

Introduction

This document gives guidelines for designing hardware to reside on the Amiga expansion bus. The Amiga expansion bus is a relatively straightforward extension of the 68000 bus.

Hardware for the bus can be viewed as two categories: backplanes and PICs. Backplanes interface to the 86-pin connector of either another backplane or the Amiga itself. Backplanes buffer the bus and provide 100-pin connectors for PICs to plug into.

PIC is an acronym for plug-in card. A PIC is usually a card that plugs into the standard 100 pin Amiga backplane (as defined in this document).

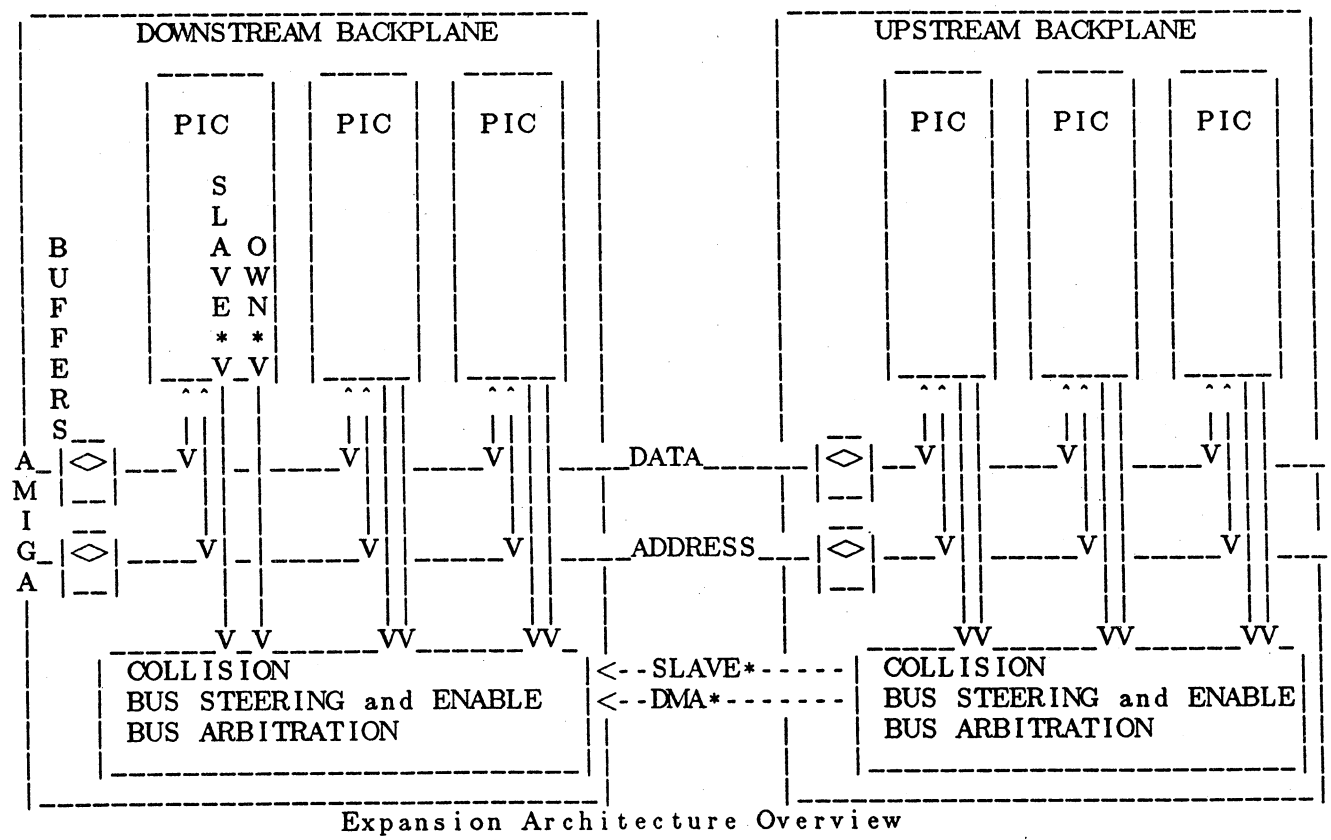
A sub-type of PIC is a combination of backplane and PIC integrated into one package. These combination products should follow all of the applicable backplane and PIC rules, especially auto-configuration.

Software never sees backplanes, all expansion hardware appears to the software as PICs.

1. Expansion Architecture Overview

As shown in the figure "Expansion Architecture Overview," the expansion bus is implemented as daisy-chained backplanes (expansion boxes) which accept PICs (boards). For timing and FCC reasons, it is probably not feasible to configure a system with more than two external backplanes attached. Even with only two, the timing is very tight, so the designer must be careful.

This document attempts to address the worst case, which is designing PICs and backplanes that are fast enough to use two such backplanes daisy-chained. It should be noted that a similar box that is designed to be the only backplane on the system could make some reductions in speed requirements and logic complexity.



Expansion Architecture Overview

Due to timing considerations it is not possible to daisy chain more than two buffered backplanes without inserting wait states.

2.1.5. List of Signals on 86-Pin and 100-Pin Connectors

Appendix X lists all signal names on the 86 and 100 pin connectors. Note: If appendix X is not in this document yet, see accompanying schematic of backplane for pin lists.

List of signals that are unique to each connector.

List of signals that are on 100 pin conn but not on 86 pin

Describe function of each Amiga specific signal, eg SLAVE*, DMAOUT*, ASDELAYED*, 7M, OWN*, others?

2.2. The Protocols

The bus protocols are basically the same as standard 68000 protocols, however the timing margins are tighter due to the potentially long paths of Amiga and PICs talking to each other across two buffered backplanes.

One unusual feature is that when you are doing a DMA transfer into or out of the Amiga display RAM (the half megabyte starting at address 000000), the DTACK* circuit will synch the master up with C1. Because C1 is twice as slow as 7M, there are two possible phase relationships between C1 and the beginning of the DMA bus cycle. If AS* is asserted during the last quartile of C1 (C1 low and C3 low, see clock timing diagram), we call this an "in sync" bus cycle, and DTACK* will be given in time to do a normal 4-clock (7M) bus cycle (Note: occasionally DTACK* will be delayed due to contention with the graphics chips also, but that does not matter in this discussion).

However DTACK works differently if the DMA controller asserts AS* in the other phase. In the second quartile (C1 high and C3 high) the DTACK* circuit will hold off DTACK* long enough to insert one wait state, thus syncing up the "out of sync" bus cycle.

2.2.1. Read or Write Cycle with Amiga as Master

Since the Amiga bus master is a 68000, the bus cycle is a 68000 cycle. However, the responding slave does not pull DTACK*. Our internal circuitry will pull DTACK* unless the slave pulls XRDY low.

Also, the slave (PIC) must pull its SLAVE* output low as soon as it is selected, and at the end of the cycle disassert SLAVE* when AS* goes away.

2.2.2. Read or Write Cycle with a PIC as Master

A PIC as master must drive the bus using the same protocol as the 68000. Some of the timing margins must be better than those from the 68000, because the PIC is driving through several levels of buffers, and the Amiga logic is designed to the 68000 (8 megahertz part) specs. Specific timing requirements can be found in the tables in the timing appendix (Appendix A).

2.2.3. Bus Arbitration

The bus arbitration scheme is based on the 68000 BR*,BG*,BGACK* protocol. PICs are required to assert BR* clocked by the rising edge of 7M. This makes it less expensive to design bus arbitration logic that will be reliable. Specifically, synchronous arbitration logic can be clocked on 7M without danger of going metastable.

2.3. Timing General Discussion

See appendix A for timing specifications.

There are two main problems to be dealt with in the expansion architecture timing: propagation delays and skews in the clock, address, data, and control paths. The timing is tight, thus we recommend using FAST and AS parts to buffer these lines. To guarantee meeting the timing requirements, you must be careful to not exceed the recommended operating conditions of the parts you chose, for example the capacitive loading. In calculating your loading, note that all PICs are specified to present no more than two "F" loads plus minimal trace capacitance to each connector pin. Backplanes are specified to present no more than one "F" load plus trace capacitance to the Amiga. Do not use "typical" numbers, reliable systems can be built by using "worst case" numbers.

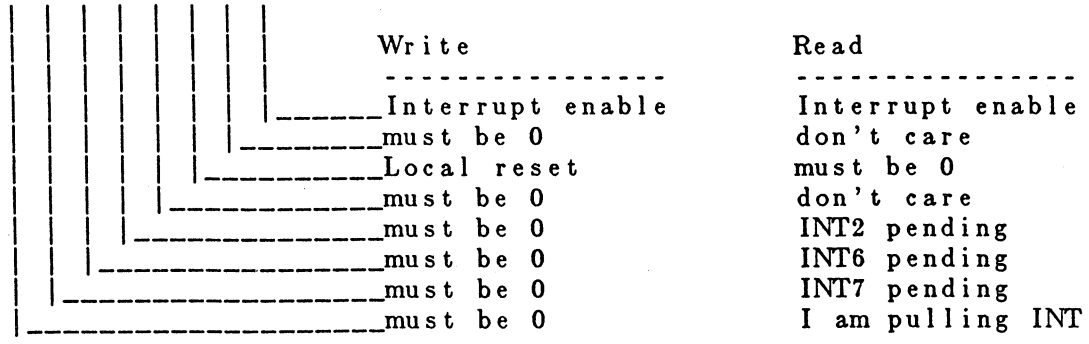
Appendix A gives the timing required in order to meet the timing requirements of two buffered backplanes with PICs.

(20/22)	7 6 5 4 3 2 1 0	Optional serial number, byte 2
(24/26)	7 6 5 4 3 2 1 0	Optional serial number, byte 3 (lsb)
(28/2A)	7 6 5 4 3 2 1 0	Optional init/diagnostic vector high byte
(2C/2E)	7 6 5 4 3 2 1 0	Optional init/diagnostic vector low byte
(30/32)	7 6 5 4 3 2 1 0	Reserved, must be 0
(34/36)	7 6 5 4 3 2 1 0	Reserved, must be 0
(38/3A)	7 6 5 4 3 2 1 0	Reserved, must be 0
(3C/3E)	7 6 5 4 3 2 1 0	Reserved, must be 0
(40/42)	7 6 5 4 3 2 1 0	Optional control status register
(44/46)	7 6 5 4 3 2 1 0	Reserved, must be 0
(48/4A)	7 6 5 4 3 2 1 0	Base address register
(4C/4E)	x x x x x x x x	Optional ''shut up'' address
(50/52)	7 6 5 4 3 2 1 0	Reserved, must be 0
(54/56)	7 6 5 4 3 2 1 0	Reserved, must be 0
(58/5A)	7 6 5 4 3 2 1 0	Reserved, must be 0
(5C/5E)	7 6 5 4 3 2 1 0	Reserved, must be 0
(60/62)	7 6 5 4 3 2 1 0	Reserved, must be 0
(64/66)	7 6 5 4 3 2 1 0	Reserved, must be 0
(68/6A)	7 6 5 4 3 2 1 0	Reserved, must be 0
(6C/6E)	7 6 5 4 3 2 1 0	Reserved, must be 0
(70/72)	7 6 5 4 3 2 1 0	Reserved, must be 0
(74/76)	7 6 5 4 3 2 1 0	Reserved, must be 0
(78/7A)	7 6 5 4 3 2 1 0	Reserved, must be 0
(7C/7E)	7 6 5 4 3 2 1 0	Reserved, must be 0

Descriptions:

(00/02) 7 6 5 4 3 2 1 0 — Board type and size

- bits 7-6: Memory size
  - 000 = 8 megabytes
  - 001 = 64 kilobytes
  - 010 = 128 kilobytes
  - 011 = 256 kilobytes
  - 100 = 512 kilobytes
  - 101 = 1 megabytes
  - 110 = 2 megabytes
  - 111 = 4 megabytes
- bit 5: Chained config request, indicates that the next auto-config device in the daisy chain is physically tied to this device.
- bit 4: Diagnostic address valid
- bit 3: Link into memory free list



(44/46) 7 6 5 4 3 2 1 0 Reserved

Write	Read
Not defined	must be 00

% Neil - what is this?

(48/4A) 7 6 5 4 3 2 1 0 Base address register, write-only

These bits are compared with A23 through A16 (or fewer) to determine the base address of this board.

(4C/4E) x x x x x x x x Optional ''shut up'' address, a write to this address will cause the board to pass its config out and then never again respond to any address. RESET will re-enable the board. The actual address that has this effect is 4C. A write to 4E is ignored. This is write only.

(50/52)	7 6 5 4 3 2 1 0	Reserved, must be 00
(54/56)	7 6 5 4 3 2 1 0	Reserved, must be 00
(58/5A)	7 6 5 4 3 2 1 0	Reserved, must be 00
(5C/5E)	7 6 5 4 3 2 1 0	Reserved, must be 00
(60/62)	7 6 5 4 3 2 1 0	Reserved, must be 00
(64/66)	7 6 5 4 3 2 1 0	Reserved, must be 00
(68/6A)	7 6 5 4 3 2 1 0	Reserved, must be 00
(6C/6E)	7 6 5 4 3 2 1 0	Reserved, must be 00
(70/72)	7 6 5 4 3 2 1 0	Reserved, must be 00
(74/76)	7 6 5 4 3 2 1 0	Reserved, must be 00
(78/7A)	7 6 5 4 3 2 1 0	Reserved, must be 00
(7C/7E)	7 6 5 4 3 2 1 0	Reserved, must be 00

3.4. Mechanical

Two mechanical drawings are included in this package. The first gives the physical dimensions and pin locations for a PIC board.

The second gives detailed dimensions of the 86-pin expansion connector on the right side of the Amiga.

Board center to top of highest component should not exceed .60 inches on PICs. The backplane should provide a minimum of .80 inches center to center for the boards.

DMAOUT = DMAIN + OWN

DMAIN is active when the bus master is upstream from this backplane. So when DMAIN is active, DMAOUT must go active.

OWN* is the wire OR'ed signal which means that this backplane has the current bus master. Thus because all PICs on this backplane are upstream from the address (and data) buffers, DMAOUT must be active when OWN (or OWN*) is active.

4.2.1.2. Generating ADDR_OE*

This section explains the PAL equation for ADDR_OE*. Refer to the "STEERING PAL" appendix to see the equation (AOE).

ADDR_OE* is active (enabling the address drivers) most of the time. It only disables the drivers when ownership of the bus is changing (for example a new master takes control). At these transition times ADDR_OE* is inactive so that the tri-state drivers will not fight the drivers on the next backplane while they are changing direction.

Refer to the equation for AOE in the "STEERING PAL" appendix. AOE = ADDR_OE* inverted. The inverter is in the output stage of the PAL.

BGACK is asserted (BGACK* pulled low) by all bus masters (except the 68000) when they are the current master, so ADDR_OE* is active when BGACK is active.

The term (BG* * DMAOUT*) is true most of the time that the 68000 owns the bus. However, when the 68000 is about to give up the bus, BG* will go active and thus (BG* * DMAOUT*) will go inactive. It is important that the address drivers remain on until the end of the final 68000 bus cycle when the 68000 is giving up the bus, so the term AS holds AOE active when BG goes active during the bus cycle.

AS does not last quite long enough, so ASQ90 (which is a slightly delayed AS) holds AOE active long enough to finish the cycle.

4.2.2. The Data Buffers

This section describes when and why the data drivers are turned on and off. It also describes control of data direction.

4.2.2.1. Generating DBOE*

Refer to the STEERING PAL equation for DBOE.

Note that all the bus drivers are enabled for every bus cycle unless BERR* is asserted. This allows for easier use of bus-monitoring tools such as state analyzers.

It is fairly difficult to avoid tri-state fights on the data buffers. In order to get data out to dynamic RAM PICs at an early enough time, we do not use the data strobes to enable the data drivers, because these strobes can go active very late in a write cycle.

On a read cycle we use the data strobes, so that in case the cycle turns out to be a Read-Modify-Write cycle, the drivers will be turned off (to avoid tri-state fight) while the R/W line is changing state.

Refer to the PAL equation for DBOE in the STEERING PAL appendix. The term (AS * RD*) turns on the drivers for all write cycles, including the write portion of Read-Modify-Write cycles. Note that since AS turns off the data drivers, the data hold time is not guaranteed beyond AS going inactive, so it is poor design practice to try to use the rising edge of AS*, UDS*, or LDS* to latch data.

The terms (UDS * RD * ASQ) and (LDS * RD * ASQ) turn on the drivers for all read cycles. The UDS and LDS turn off the drivers in the middle of a read-modify-write cycle. Note that since AS turns off the data drivers, the data-hold time is not guaranteed beyond AS going inactive. Therefore it is poor design practice to try to use the rising edge of AS*, UDS*, or LDS* to latch data.

The terms (UDS * RD * ASQ) and (LDS * RD * ASQ) turn on the drivers for all read cycles. The ASQ (ASDELAYED equivalent) keeps the data buffers from turning on until after there has been enough time for the collision

4.4. Bus Arbitration Circuit

The bus arbitration circuit's main job is to determine which PIC will receive BG* active (Bus Grant) when the 68000 asserts BG*. The circuit we recommend does this based on priority, where the closest PIC to the 68000 is the highest priority. You could implement something fancier as long as only one PIC owns the bus at a time.

PICs are only allowed to assert BR* off the rising edge of 7M. This allows the bus arbitration circuit to operate synchronously, clocked by the rising edge of 7M.

The output of the bus arbitration circuit only changes when the 68000 changes the state of BG*. If the 68000 is asserting BG*, the arbitration circuit passes BG* active to the highest priority active requester. When the 68000 disasserts BG*, the arbitration disasserts BG* also. Therefore no PIC has a grant.

4.5. RES* and RESB*

Note that there are two reset lines going to every PIC, RES* on pin 53 and RESB* on pin 94. The RESB* line is intended to be the normal reset input to the PIC. All normal PICs will use this line as an input, so it is buffered.

RES* is intended only to be used by those PICs which are designed to have the capability of reseting the system. Normal PICs will not drive nor load this line. Note that because RES* is not buffered, it can reset the Amiga, as well as resetting all PICs (via RESB*).

4.6. CONFIG_IN* CONFIG_OUT* Daisy Chain

The CONFIG_IN* signal will be passed to CONFIG_OUT* at the appropriate time if there is a PIC plugged in the slot. On this backplane, we have used 74LS32s to pass CONFIG_OUT* to the next slot if there is no PIC. The pull down resistor allows the CONFIG_IN* signal to pass directly through the gate to CONFIG_IN* of the next slot if there is no PIC installed, thus bypassing the empty slot. If a PIC is installed, the PIC's CONFIG_OUT* driver will override the pull down resistor.

Another method that would work is to use special pins on the connector at pins 11 and 12, such that 11 and 12 short to each other when there is no PIC inserted in the connector. This would eliminate the need for the 74LS32 gates.

4.7. Backplane Timing Generation

4.7.1. Clock Buffers

The clock buffers for C1*, C3*, and CDAC were chosen for minimum propagation delay and minimum skew. Notice that buffered clocks are passed to the 100 pin edge connectors, but that the unbuffered clocks are passed to the 86 pin connector that goes on to the next box in order to minimize propagation delay to the next backplane.

4.7.2. Generating 7M

We generate 7M (equivalent to the processor clock) by:

7M = C1* XNOR C3*

This yields a 7.16Mhz clock which is used to generate ASDELAYED*, DOE, and ASQ90*. 7M is also passed to the PICs on pin 92 of the edge connectors, so they will have a cheap clock for accessing the bus.

4.7.3. DOE, ASDELAYED*, ASQ90*

DOE (Data output enable) and ASDELAYED* are the compliment of each other. ASDELAYED*is used in the steering PAL (ASQ = ASDELAYED in the PAL equations) to time turning on of the data drivers during a read cycle. DOE is passed to the PICs on pin 93 of the edge connectors, to tell the PICs when to turn on data drivers during a read cycle.

Notice that whenever BOARD_SEL* goes active, SLAVE* will go active unless SHUT_UP_FOREVER is latched active. SHUT_UP_FOREVER* is a feedback latch in the PAL. It is only set by the software if the board cannot be configured into the system (for instance if the user has plugged in too many large address space PICs and there is no room left for this one).

If you analyze the PAL equations for BD15 through BD12, you will see that their data drivers turn on for all reads ANDed with BOARD_SEL active, until CONFIG_OUT* is set active (or some exception happens such as reset, bus error, or shutup).

By the way, if you're not used to PALs, it's normal old Boolean: * means AND, / is bar, + is OR, IF(term) means "If the term evaluates to TRUE then turn on the tri-state driver".

Further analysis of the BD15-BD12 equations will show that almost all addresses put out ones; however, remember that most of the nibbles are inverted because the spec says they have to be (not all of course, noooo that would be too simple.) The inversion makes it possible to implement the codes in active low PALs; it is just a cost reduction.

Analysis of the equations shows that the only nibbles (we don't care about above HEX 80) that are outputting any zeros are:

```
00/02  1100 0001
04/06  1111 1001
10/12  1111 1110
40/42  0000 0000
```

To interpret this code, we need to remember that the spec says that all nibbles get inverted except 00, 02, 40, and 42. So our new table looks like this:

```
00/02  1100 0001
04/06  0000 0110
10/12  0000 0001
40/42  0000 0000
```

And all the other nibbles that were ones are now inverted to zeros.

What do these codes mean?

```
Nibble     Data
00/02      1100 0001
           ||||_||_|________001 = 64 kilobytes, the smallest size that can
           ||||  |                can be requested
           ||||  |
           ||||  |______________0 = There are no more PICs on this physical
           ||||                   board. It is possible to put more than
           ||||                   one PIC on a physical board, but in
           ||||                   most cases including this one, we don't.
           ||||
           ||||_________________0 = This board does not have any Init or
           |||                    diagnostic code.
           |||  .
           |||__________________0 = Don't link into memory free list. The
           ||                     reason I didn't want it linked in is that
           ||                     the processor might have tried to use it
        ||                      and it was only 16 kilobytes masquerading to
           ||                     the system as 64 kilobytes.
           ||
           ||
           ||__________________11 = Required by the spec.

04/06      0000 0110___________ = Product number = 6

10/12      0000 0001___________ = High byte of manufacturers number
14/16      0000 0000___________ = Low byte of manufacturers number
```

Guaranteed Timing to Backplane				
Num	Characteristic	Min	Max	Unit
1	AS* Low to CDAC low (Setup)	20		ns
2	AS* High to CDAC High (Setup)	20		ns

6.4. Guaranteed Timing to PIC

Guaranteed Timing to PIC (PIC in Slave Mode)				
Num	Characteristic	Min	Max	Unit
1	Valid Address to AS* Low	10		ns
2	Valid Data from 7M High(S4) on Wr to PIC		35	ns

Guaranteed Timing to PIC (PIC in Master Mode)				
Num	Characteristic	Min	Max	Unit
1	Valid Data setup to Local 7M low(S7)	15		ns

7. Appendix B - Backplane Loading Spec

Note: The Amiga is designed to drive into a device that meets the backplane specification.

% need to spec how many pf a box may present to the upstream box

All backplane 86-pin connectors at the processor end of the backplane must present no more than 1 "F" load plus ??pf to the connecting device, with the following exceptions:

Pin 53 RES*

7.1. Appendix C - PIC Loading Spec

All PIC pins must present no more than 2 "F" loads plus trace capacitance.

7.2. Appendix D - Clocks

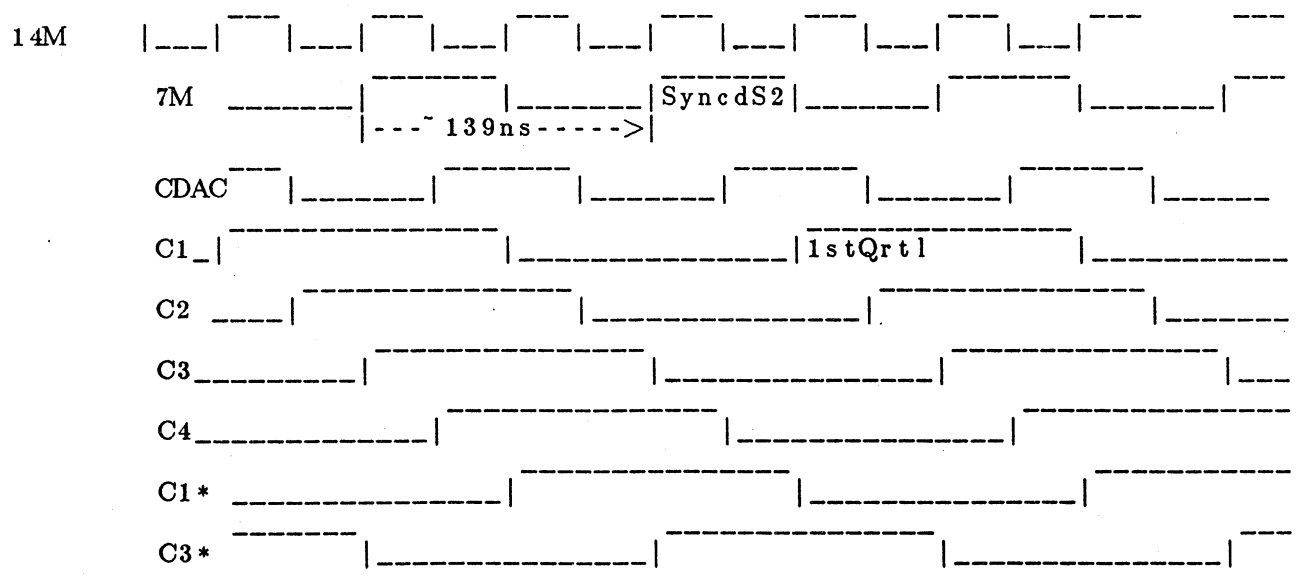


Fig. 1 Amiga System Clocks

```
PAL16L8
STEERING15OR17 REV3
11-17-85
AMIGA

/SLVOUT RD /ASQ /ASQ90 COLLIS /BG /AS /BGACK /DMAIN GND
/OWN /AOE /UDS /BERR /DMAOUT /LDS /DBOE /RES /D2P VCC


DBOE    = AS   * /RD        * /BERR +          ;DATA DRIVERS DURING WRITE CYCLE
          UDS *  RD * ASQ   * /BERR +          ;TURN ON DRIVERS LATE FOR RD
          LDS *  RD * ASQ   * /BERR            ;UDS AND LDS PROTECT RD MOD WR
                                               ;TO AVOID TRI_STATE FIGHT
D2P     = /DMAOUT *  SLVOUT *  RD +            ;DOWNSTREAM READS UPSTREAM SLAVE
           DMAOUT * /SLVOUT * /RD +            ;UPSTREAM WRITES DOWNSTREAM SLAVE
           DMAOUT *  SLVOUT                    ;MASTER AND SLAVE ARE UPSTREAM

AOE     = BGACK          +
          /BG * /DMAOUT  +
          AS             +                    ;AS KEEPS ADDR WHEN /BG DROPS
          ASQ90                               ;ASQ90 MAINTAINS VALID ADDR ON
                                               ; LAST PROC CYCLE

DMAOUT = DMAIN + OWN

IF (/RES * COLLIS) BERR = VCC

DESCRIPTION

SLVOUT=SLAVEOUT,ASQ=AS DELAYED,ASQ90=AS CLKD ON LOW EDGE OF 7M,
BG=BUS GRANT,OWN=LOCAL OWN
COLLIS=BUS COLLISION,AOE=ADDR OUTPUT EN,DOE=DATA OE
RES=RESET,D2P=DATA TO PROCESSOR
UDS LDS PROTECT AGAINST RDMODIFYWRITE 3STFIGHT & BERR= /DOE
```

```
PAL20L10
TESTRAM
9-11-85
COMMODORE-AMIGA

/ASQ /ASQQ RD /BDSEL /BERR A6 A5 A4 A3 A2
A1 GND /RES BD12 BD13 BD14 BD15 /PRECON /CONOUT /SHUTUP
/RAMOE /WP /DBOE VCC

DBOE = /RES*BDSEL*/BERR*/SHUTUP*/RD +                    ;WRITES TURN ON EARLY
       /RES*BDSEL*/BERR*/SHUTUP* RD*ASQ                  ;ASQ DELAYS THE READ

WP   = /RES*ASQ*/ASQQ*BDSEL*CONOUT*/SHUTUP*/RD*/BERR

RAMOE = /RES*ASQ*RD*CONOUT*/BERR*BDSEL

SHUTUP = /RES*BDSEL*/RD*ASQ*/CONOUT*A6*/A5*/A4*A3*A2 +
         /RES*SHUTUP

PRECON = /RES*SHUTUP +
         /RES*/RD*BDSEL*ASQQ*A6*/A5*/A4*A3*/A2*/A1 +
         /RES*PRECON

CONOUT = /RES*/ASQ*PRECON +
         /RES*CONOUT

IF(/RES*BDSEL*/CONOUT*RD*/BERR*/SHUTUP) /BD15 =
         /A6*/A5*/A4*/A3*/A2*A1 +
          A6*/A5*/A4*/A3*/A2

IF(/RES*BDSEL*/CONOUT*RD*/BERR*/SHUTUP) /BD14 =
         /A6*/A5*/A4*/A3*A1 +
          A6*/A5*/A4*/A3*/A2

IF(/RES*BDSEL*/CONOUT*RD*/BERR*/SHUTUP) /BD13 =
         /A6*/A5*/A4*/A3*/A2 +
         /A6*/A5*/A4*/A3*A2*A1 +
          A6*/A5*/A4*/A3*/A2

IF(/RES*BDSEL*/CONOUT*RD*/BERR*/SHUTUP) /BD12 =
         /A6*/A5*/A4*/A3*/A2*/A1 +
         /A6*/A5*A4*/A3*/A2*A1 +
          A6*/A5*/A4*/A3*/A2

DESCRIPTION

THING
```

INTERFACING TO THE 68K BUS CONNECTOR ON THE AMIGA

0. Scope

WARNING: While care has been taken to make this document as accurate as possible, it is preliminary and is subject to change without notice.

This document is intended to give the necessary information for interfacing to the 68000 bus connector on the right side of the Amiga computer. It will be updated as people give feedback.

0.1 References

The Amiga Hardware Manual gives the address map and other useful information.

Appendix E of the hardware manual gives the complete pinout for the 86 pin connector.

1. Form Factors

1.1 Form Factors For Standard Box With Cards

We are planning on recommending a standard form factor for motherboards and daughter cards for the Amiga. While this definition is not yet solid, we have some preliminary information. See attached drawing for the proposed daughter card form factor.

1.2 The Connector On The Amiga

The connector is a standard dual row 86 finger (43 on a side) edge connector, spaced on .1" centers. Here are some part numbers of connectors that are compatible:

solder tail	AMP 2-530841-1
wire wrap	AMP 4-530396-7
card extender	AMP 1-530826-2

Mitsumi also makes connectors that fit.

See accompanying drawing for physical dimensions of this connector.

2. Timing

2.1 Clocks

For this discussion see figure 1.

The entire computer board is run synchronously to the 3.57954Mhz color clock (C1). This is accomplished by generating a number of sub-multiple frequencies from our master 28.63636Mhz crystal oscillator. The following are the primary clocks on the board:

The 68000 is connected directly to the 86 pin connector, there are no buffers between the 68000 and the connector. Two control inputs, VPA* and DTACK* are driven by logic on the Amiga and should not be driven by your circuitry.

Many boxes are being designed which pass the bus (buffered) out in daisy chain fashion.
In order to allow your device to be the second in the chain, you must take into account an extra level of signal buffers on:

AS*, UDS*, LDS*, Address, Data, Clocks

We will be publishing guidelines on how to design compatible expansion boards, so that boards and boxes from various companies will be able to coexist on the bus. One of the requirements will probably be that data drivers should not be enabled until early in S4 on a Read cycle.

Futhermore, if you are designing a DMA device, the Amiga provides data in response to a Read very late (approx 50ns prior to the fall of S6). If your DMA device is looking at this data through two or three 74F245's (7ns each), this data will not be valid at your DMA controller until approximately 25ns prior to the fall of S6.

Our bus timing is based on an 8Mhz 68000, with only one exception: under normal operation our bus control PAL will assert DTACK* for you. DO NOT ASSERT DTACK*; do not attach any outputs to the DTACK* line.

2.21 Slave Bus Timing

Details of 68000 timing are available in the Motorola 68000 hardware manual. If you are designing a bus slave, most bus timing is per the 68000 spec, except that we will pull DTACK* for you. If you need to delay our assertion of DTACK*, you must pull XRDY (Pin 18) no later than 60ns after the assertion of AS*. You should release XRDY when you are ready to complete the bus cycle.

Also remember that in the expansion architecture, data drivers should not turn on during a Read cycle until S4.

For those of you who have not designed anything on the 68K bus before, this description is intended to make looking at the Motorola timing diagrams easier. For more details and timing specs see Motorola hardware manual (fold out timing diagrams in the back of the book.)

See figure 2 in this document.
Motorola labels the states of the processor clock S0-S7. The processor starts driving the address lines during S1, and asserts AS* (Address Strobe) during S2. If the cycle is a read, the data strobes (UDS*,LDS*) are asserted during S2 also (they are delayed until S4 on a write).

Our board responds to AS* by asserting DTACK* (unless you delay DTACK*

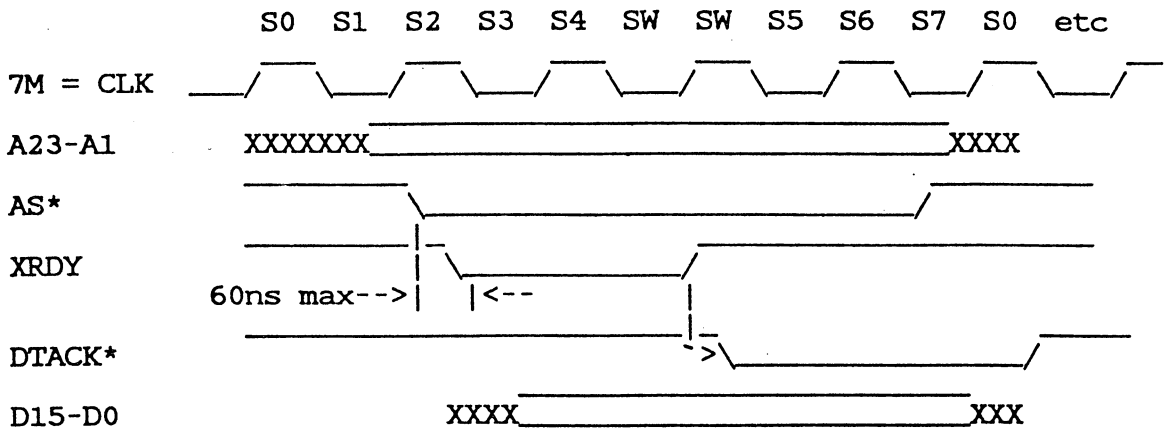


Fig. 4 Using XRDY to Delay DTACK*

2.22 Master Bus Timing

All bus masters must run synchronously to 7M (equivalent), as does the 68000 in the Amiga.

The necessary information for designing a bus master is in the 68000 hardware manual. In our system, a master must meet all of the bus timing specs of an 8Mhz 68000 , for example valid address must precede AS* by at least
30ns just as the spec says it will on an 8Mhz 68000, etc etc.

If you are designing a bus master card that will plug into a box, remember that the address will have to propagate through the address drivers that are built into the box; you should probably allow for the prop delay of three 74F245's in addition to the required 30ns.

The strobes such as AS*,UDS*,LDS* must all function as they would based on the 68000 spec. A master must also respond to DTACK*, HALT*, and BERR* correctly.

2.23 Bus Arbitration Timing

The bus arbitration logic is based on the BR* BG* OWN* BGACK* protocol as specified by Motorola in the 68000 and 68440 manuals.

All changes in state of BR* BG* and BGACK* should be clocked off the rising edge of 7M (equivalent). This allows the parallel bus arbitration logic to run synchronously to 7M without danger of clocking flip flops while these signals are changing.

The following design is for illustration, and has not been tested at this time. Notice that all state changes are synchronous to 7M and

If your slave uses the VPA VMA protocol to be synchronous with the E clock, you must only use addresses in which A12 and A13 are high. This is because we have synchronous ports on board which are activated by (A12* AND VMA), also (A13* AND VMA).

3.6 Do Not Use Pins Marked EXP

Do not drive or load pins marked EXP or RESERVE.

3.7 CONFIG*

The CONFIG* output is discussed in the Appendix (Autoconfiguration).

Only use CONFIG* as a logical input. On the first version of the Amiga it is tied to ground, but on future versions it may be driven High or Low as appropriate. Do not tie this pin to an output or to VCC or GND.

4. Loading

There is 1 AMP available on the plus 5 volts.

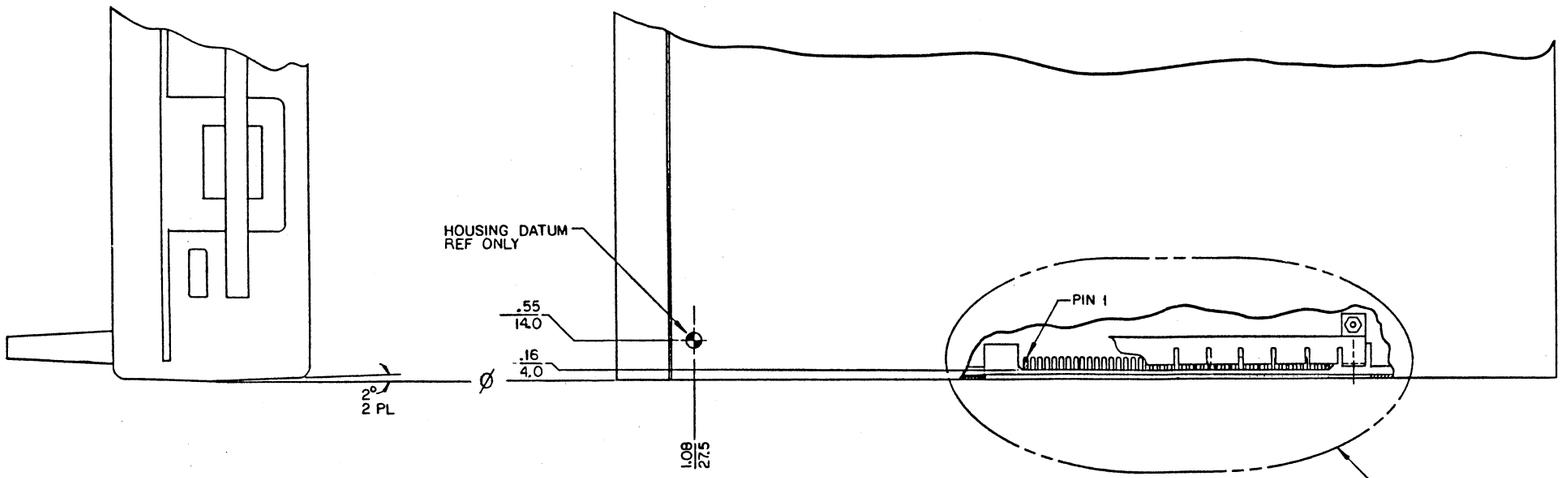
Put your buffers as close to connector as you possibly can.

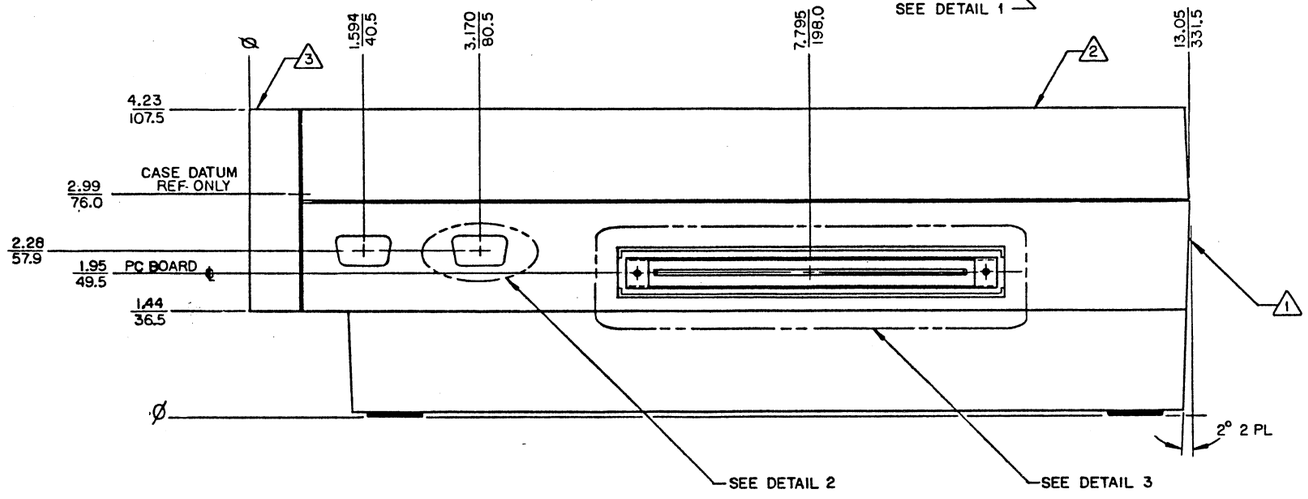
You can put one 74F load on each signal.

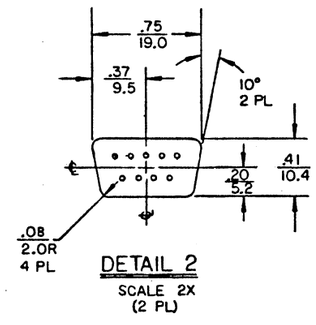
5. Warning

The Auto Configuration information in Appendix G of the Amiga Hardware Manual (Rev 1.0 8.27.85) is out of date and should not be implemented. We will soon be releasing information on the supported Auto Configuration Architecture.

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	01		9/1/85	MAS
SHT 2	02	ADDED DIMS TO EX CART. FINGERS	2/19/86	MAS







DETAIL 2
SCALE 2X
(2 PL)

NOTES:

1. 327001-01 HOUSING, BOTTOM, COMPUTER
2. 327002-01 HOUSING, TOP, COMPUTER
3. 327004-01 BEZEL, COMPUTER
4. 327049-01 CONTROL DWG, PCB, COMPUTER
5. 327038-01 RF SHIELD, EXPANSION
6. COLOR—BORG WARNER NO. 33596, LIGHT BEIGE
7. TEXTURE— BEALON BK-105B
8. TO RECEIVE M3 SELF-TAPPING SCREWS FROM EXPANSION CARTRIDGE

STEWART ENGIN'G SERVICES (408) 466-2452

UNLESS OTHERWISE SPECIFIED
TOLERANCES ON:
DECIMALS
.X ±.1 .XX ±.05 .XXX ±.010
ANGLES ±1°

		DATE
DRAWN BY:	SES	9/85
CHKD:	MAS	2/19/86
ENGR:		
APPR.		

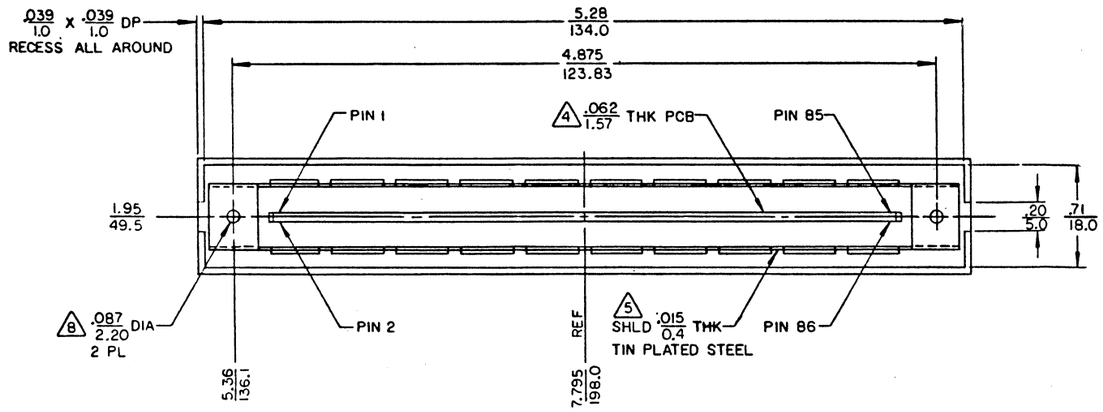
COMMODORE-AMIGA, INC.
983 UNIVERSITY AVE. #D
LOS GATOS, CA 95030

MATERIAL:
FINISH:
USED ON
NEXT ASSY

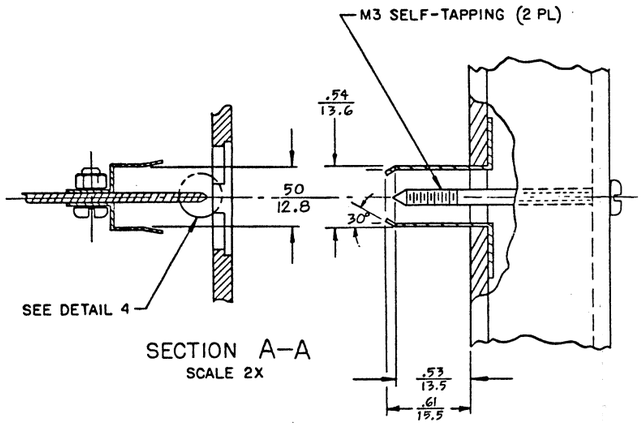
OUTLINE DRAWING
AMIGA EXPANSION

SIZE D | 327275-01 | REV 02
SCALE 1/1 | SHEET 1 OF 2

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

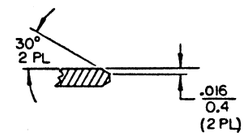


DETAIL 3
SCALE 2X

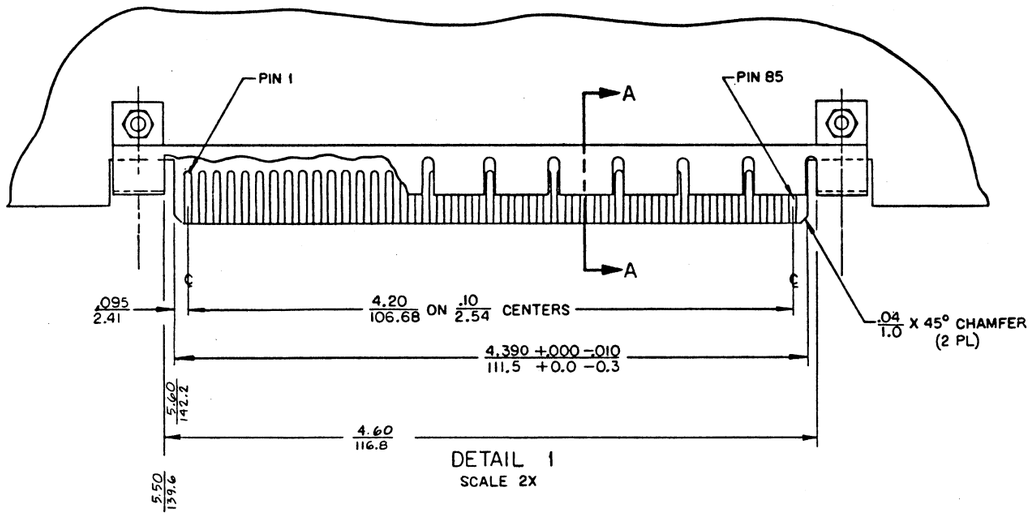


SECTION A–A
SCALE 2X

EXPANSION CARTRIDGE
(REF ONLY)



DETAIL 4
SCALE 4X



DETAIL 1
SCALE 2X

STEWART ENGIN'G SERVICES (408) 466-2452

UNLESS OTHERWISE SPECIFIED TOLERANCES ON: DECIMALS .X ±.1 .XX ±.05 .XXX ±.010 ANGLES ±1°	DRAWN BY: SES	DATE: 9-85
	CHKD	
	ENGR	
	APPR	
MATERIAL:	USED ON	NEXT ASSY
FINISH:		

COMMODORE-AMIGA, INC.
983 UNIVERSITY AVE. #D
LOS GATOS, CA 95030

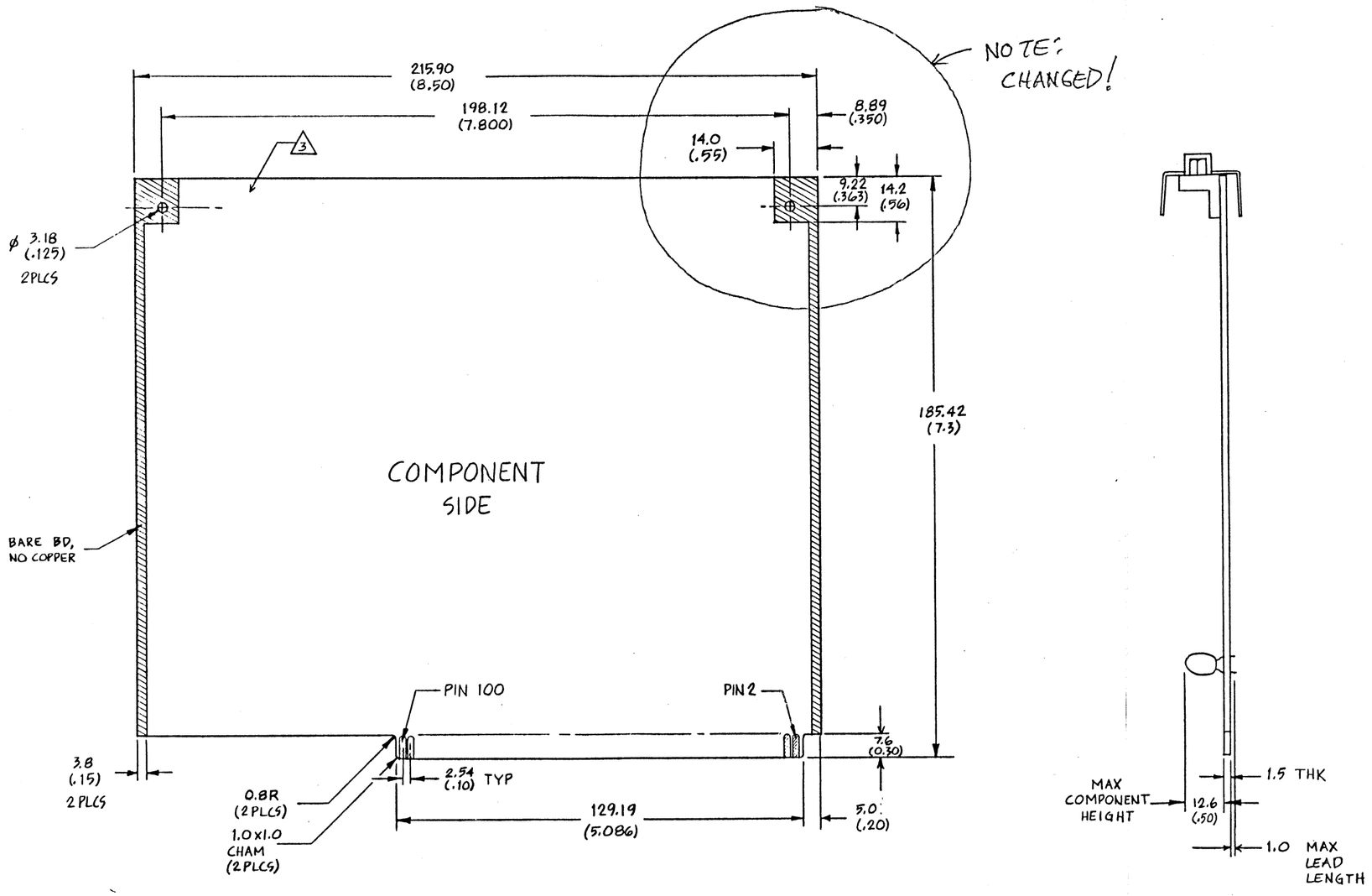
OUTLINE DRAWING
AMIGA EXPANSION

SIZE D | 327275-01 | REV 02

SCALE 1/1 | SHEET 2 OF 2

82926

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	04	REDRAWN	2/19/86	HWS
	05	129.19 WAS PLACED WRONG	3/16/86	HWS
	06	ADDED PANEL MOUNTING HOLES, CHANGED BARE COPPER AREA.		



NOTES:
1. EVEN PIN NO.S ON COMPONENT SIDE.
2. ODD PIN NO.S ON CIRCUIT SIDE.
3. ⚠3 EXTERNAL CONNECTORS ALONG THIS EDGE.

METRIC
(ENGLISH)

PRELIMINARY!

UNLESS OTHERWISE SPECIFIED
TOLERANCES ON:
DECIMALS
.X ±.4 | .XX ±.25 | .XXX ± X | ∠'S ±

DRAWN BY: HWS	DATE 2/14/86	
CHKD:		
ENGR:		
APPR:		
MATERIAL:	USED ON	NEXT ASSY
FINISH:		

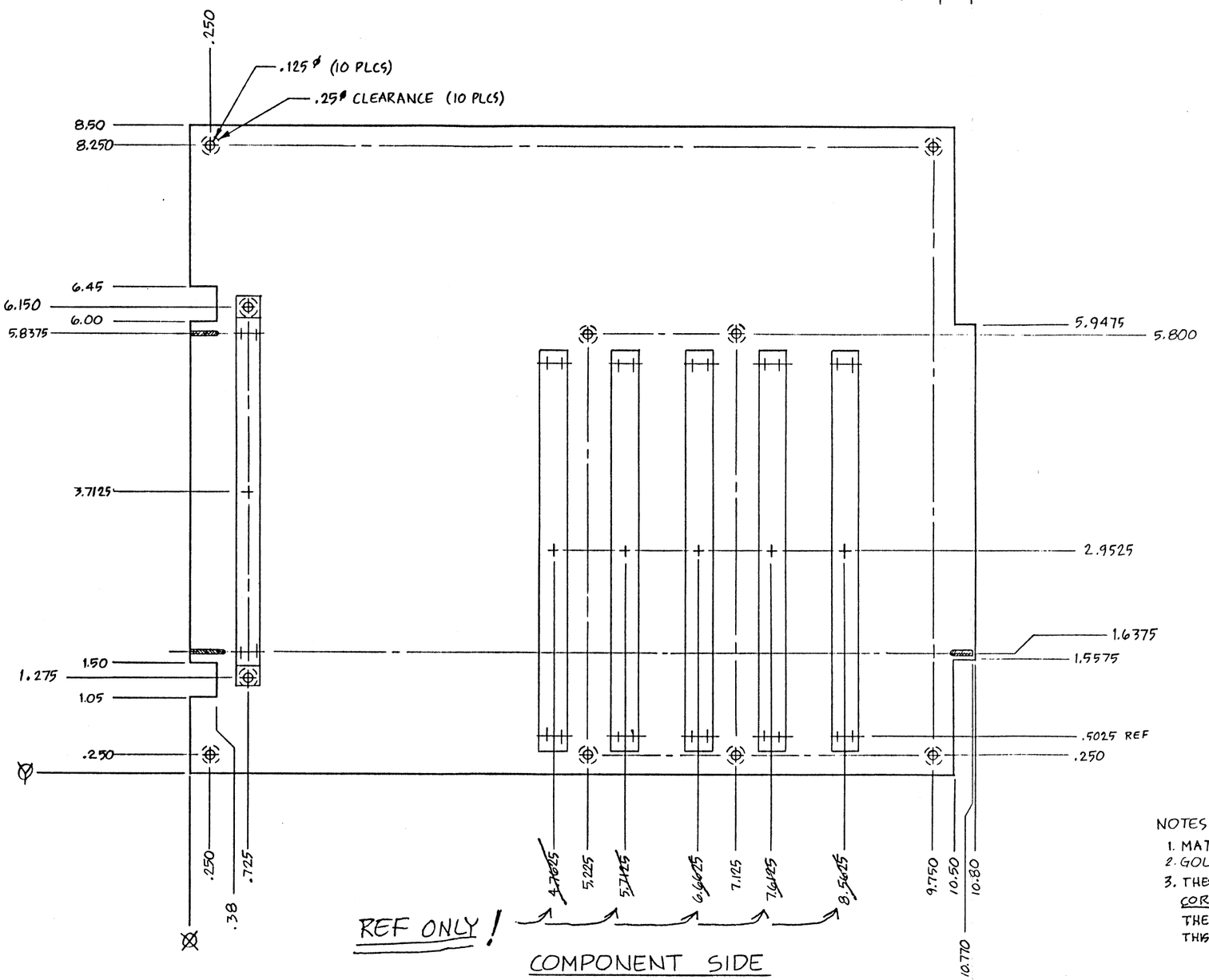
COMMODORE-AMIGA, INC.
983 UNIVERSITY AVE. #D
LOS GATOS, CA 95030

CONTROL DWG, EXPANSION BD

SIZE C | 327290-01 | REV 06

SCALE 1:1 | SHEET 1 OF 1

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED



REF ONLY!

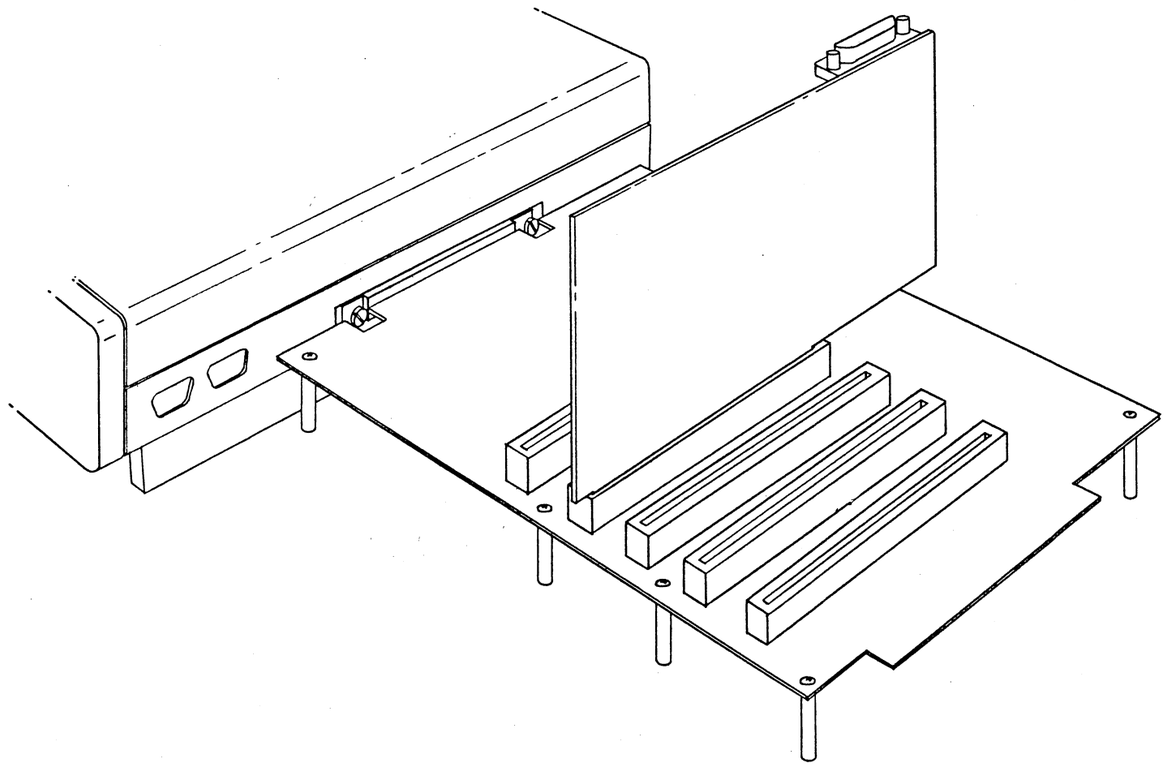
COMPONENT SIDE

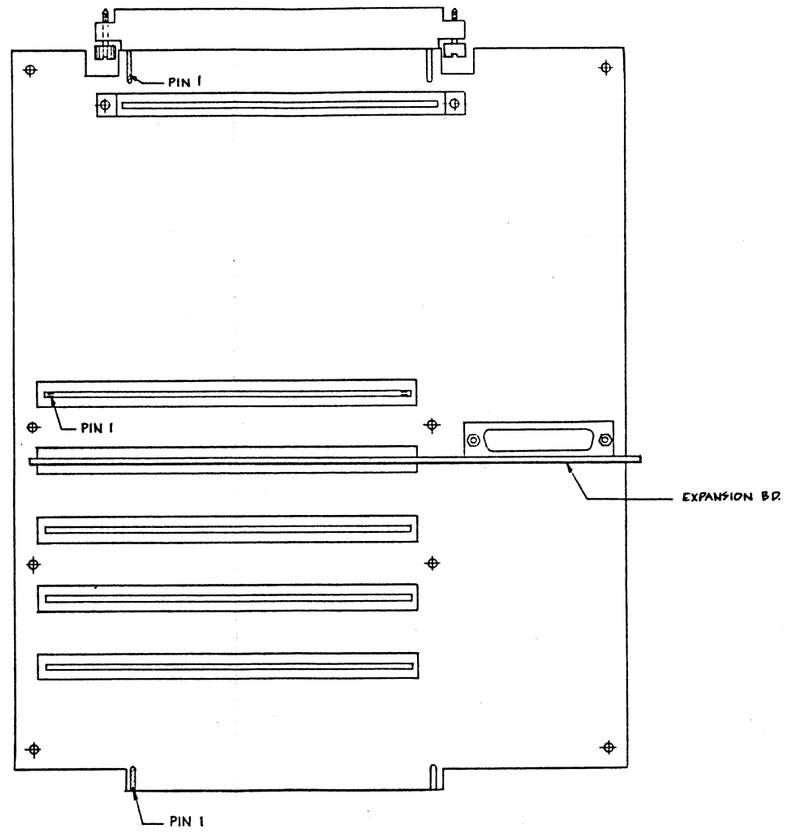
NOTES:

1. MATL: FR4 .090 THK
2. GOLD FINGERS
3. THESE DIMENSIONS ARE NOT CORRECT FOR PRODUCTION. THEY ARE TO BE USED ON THIS PROTOTYPE PCB ONLY.

UNLESS OTHERWISE SPECIFIED TOLERANCES ON: DECIMALS .X ±, .XX ±0.5, .XXX ±0.3, ∠'S ±	DRAWN BY: W WISEY	DATE 1/30/86	COMMODORE-AMIGA, INC. 983 UNIVERSITY AVE. #D LOS GATOS, CA 95030
	CHKD:		CONTROL DWG, ZORRO BACKPLANE BD.
	ENGR:		
	APPR:		
MATERIAL:	USED ON	NEXT ASSY	SIZE C 327310-01 REV 07
FINISH:			SCALE SHEET 1 OF 1

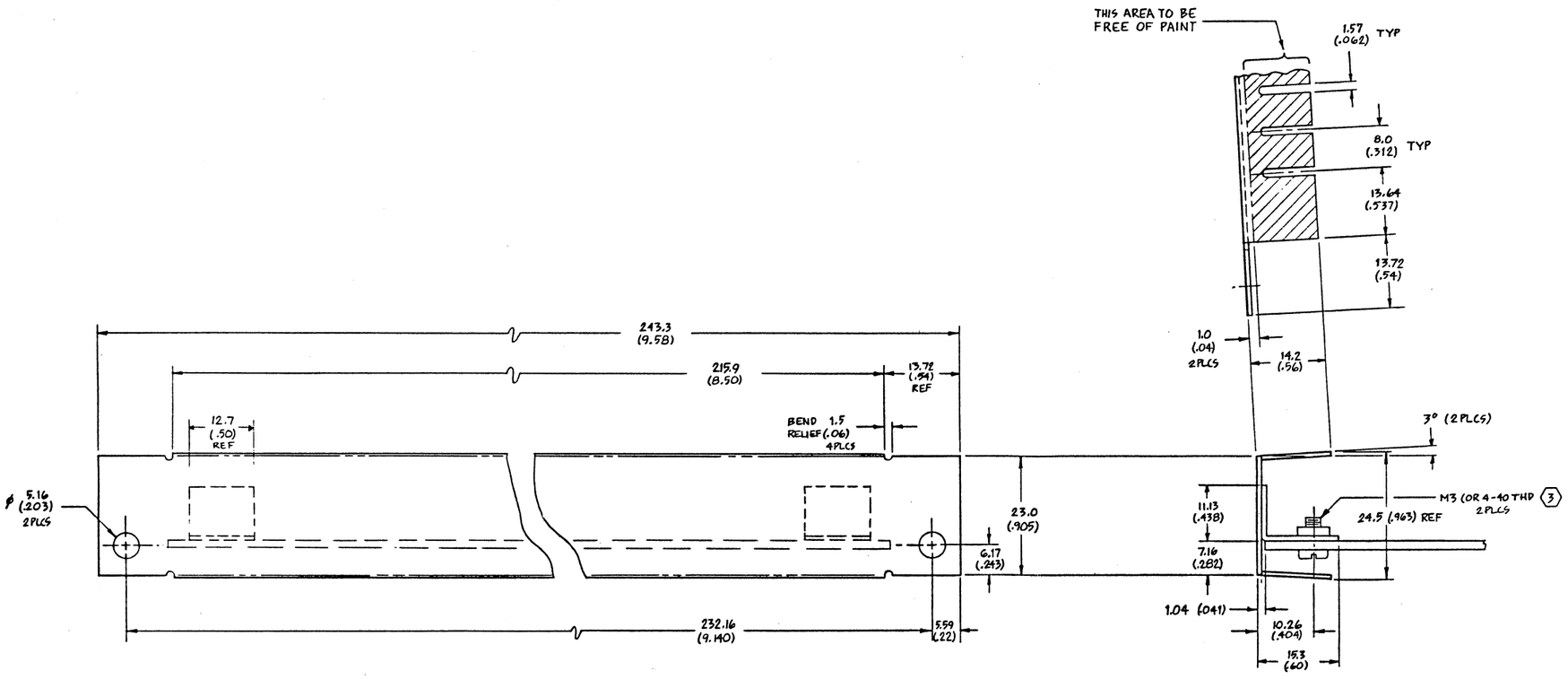
REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

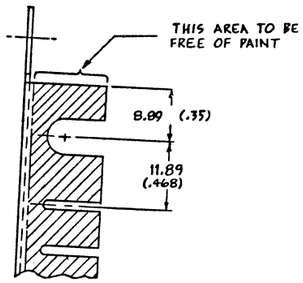


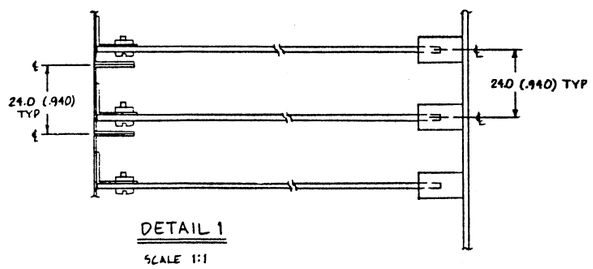


UNLESS OTHERWISE SPECIFIED TOLERANCES ON: DECIMALS .X .XX .XXX ANGLES	DRAWN BY: MJS	DATE 2/18/86	COMMODORE-AMIGA, INC. 983 UNIVERSITY AVE. RD LOS GATOS, CA 95030
	CHKD:		LAYOUT, EX. BOX
	ENGR:		
	APPR:		
MATERIAL:	USED ON	NEXT ASSY	SIZE D 327314-01 REV 01
FINISH:			SCALE SHEET 1 OF 1

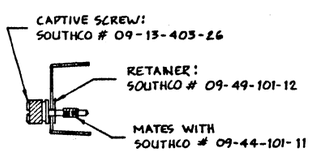
REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	01	PROTO RELEASE	4/6/86	MLS
	02	ADDED PAINT NOTE, BRKT WIDTH	4/11/86	MLS
	03	CHG'D PCB & SCREW HEIGHT	4/16/86	MLS







DETAIL 1
SCALE 1:1



DETAIL 2
2 EA REQ'D
SCALE 1:1

NOTES:
1. MATL: 0.73 (.029) THK CR STEEL, AISI 1010.
2. FINISH: PAINT - HIGH SOLIDS, POLYURETHANE BASE, SEMI GLOSS, SMOOTH COAT, CLASS-A (WHERE INDICATED) OVER CLEAR ZINC.
   COLOR - LT BEIGE: PANTONE PRO.NO. 130905.
3. PANEL SUPPORT USING 2 ANGLE BRACKETS AS SHOWN OR 2 SUB-MINI 'D' CONNRS.
4. SEE EXPANSION PCB CONTROL DWG 327290-01.

SERIOUSLY PRELIMINARY!

METRIC (INCHES)

UNLESS OTHERWISE SPECIFIED TOLERANCES ON: DECIMALS X ±0.8 (.03) XX ±0.25 (.01) XXX ±(.005) ANG ±1°	DRAWN BY: NWS	DATE 4/6/86	COMMODORE-AMIGA, INC. 983 UNIVERSITY AVE. #D LOS GATOS, CA 95030
	CHKD:		CONTROL DWG, END PANEL, EX. BD
	ENGR.		
	APPR:		
MATERIAL: SEE NOTE 1.	USED ON	NEXT ASSY	SIZE D 327335-01 REV 03
FINISH: SEE NOTE 2.			SCALE 2:1 SHEET 1 OF 1

REVISION HISTORY			
REV	ECO NUMBER	DATE	BY

WARNING

THIS PRODUCT WILL UNDERGO MAJOR REVISIONS IN THE FUTURE; THEREFORE ALL PERIPHERALS SHOULD BE DESIGNED ACCORDING TO THE INTERFACING GUIDELINES AS PROVIDED BY COMMODORE-AMIGA, INC.

COMMODORE-AMIGA, INC. RESERVES THE RIGHT TO MODIFY OR DISCONTINUE THIS PRODUCT WITHOUT NOTICE.

A CONSCIENTIOUS ATTEMPT HAS BEEN MADE TO MAKE THIS DOCUMENT ACCURATE. NO WARRANTY IS EXPRESSED OR IMPLIED.

14M
C1
C2
C3
C4
-RAS
7M
DAC
|*RAS^ |*RAS^ |*RAS^ |*RAS^ |*RAS^
| Q1 | Q2 | Q3 | Q4 |

VCC
R7 1K
SET192*
74F02
U5M
74F257
U2J
U2H
U1L
U1K
U2K-10
U2K-13
U2K-3
U2K-6
U2K-11
U2K-14
U2K-2
U2K-5
U2K-15
U2K-1
U2K-9
U2K-12
U2K-4
U2K-7
U2K-16
U2K-8
U2L-10
U2L-13
U2L-3
U2L-6
U2L-11
U2L-14
U2L-2
U2L-5
U2L-15
U2L-1
U2L-9
U2L-12
U2L-4
U2L-7
U2L-16
U2L-8
C16 0.1
C4
U5L
74LS393
U5K
74LS244
U4H
U4K
74LS373
U3H-10
U3H-20
C17 0.1
U3J
U4J
U3H-1
U3H-19
U3H-11
U3H-8
U3H-13
U3H-4
U3H-15
U3H-6
U3H-17
U3H-9
U3H-12
U3H-14
U3H-7
U3H-5
U3H-16
U3H-3
U3K-10
U3K-20
C20 0.1
U3L
U4L
U3K-1
U3K-19
U3K-17
U3K-2
U3K-9
U3K-15
U3K-4
U3K-13
U3K-6
U3K-8
U3K-11
U3K-3
U3K-18
U3K-16
U3K-5
U3K-7
U3K-14
U3K-12
U3K-9
VCC
J1 MAIN_PWR
J2
J1 MAIN_GND
J2
DPALEN
U6N
PAL16L8
U6P-1
U6P-2
U6P-3
U6P-4
U6P-5
U6P-6
U6P-7
U6P-8
U6P-9
U6P-11
U6P-28
U6P-19
C31 0.1
U6P-12
U6P-14
U6P-18
U6P-17
U6P-16
U6P-15
U6P-13
DAUGEN
U6L
DPALCAS
U6K
U6Q-7
U6Q-2
U6Q-3
U6Q-4
U6Q-5
U6Q-6
U6Q-8
U6Q-11
U6Q-13
U6Q-20
U6Q-10
U6Q-19
U6Q-14
U6Q-18
U6Q-17
U6Q-15
DAUGCAS
U6J
U6Q-12
J3 A18
J3 A17
C1*
A17
74F139
U1H
J1 RAS*
RN 33
R3 33
R5 33
R2 33
R6 33
R1 33
U2F 33x8_DIP
RN1 470x9_SIP
U2E
U1E
U2D
U1D
U2C
U1C
U2B
U1B
J1 -RESET
SROM*
R8 1K
SET_ROM*
R8 220

C2,C3,C4,C5,C6,C7,C8,C9 .22
C1 10/16 TANT
C10,C11,C12,C15,C18,C19,C21,C22,C23,C24,C26,C27,C28,C98 0.1
C13,C25 100/16

RAM_ARRAY

COMMODORE-AMIGA INC.
983 UNIVERSITY AVE.#D
LOS GATOS, CA 95030

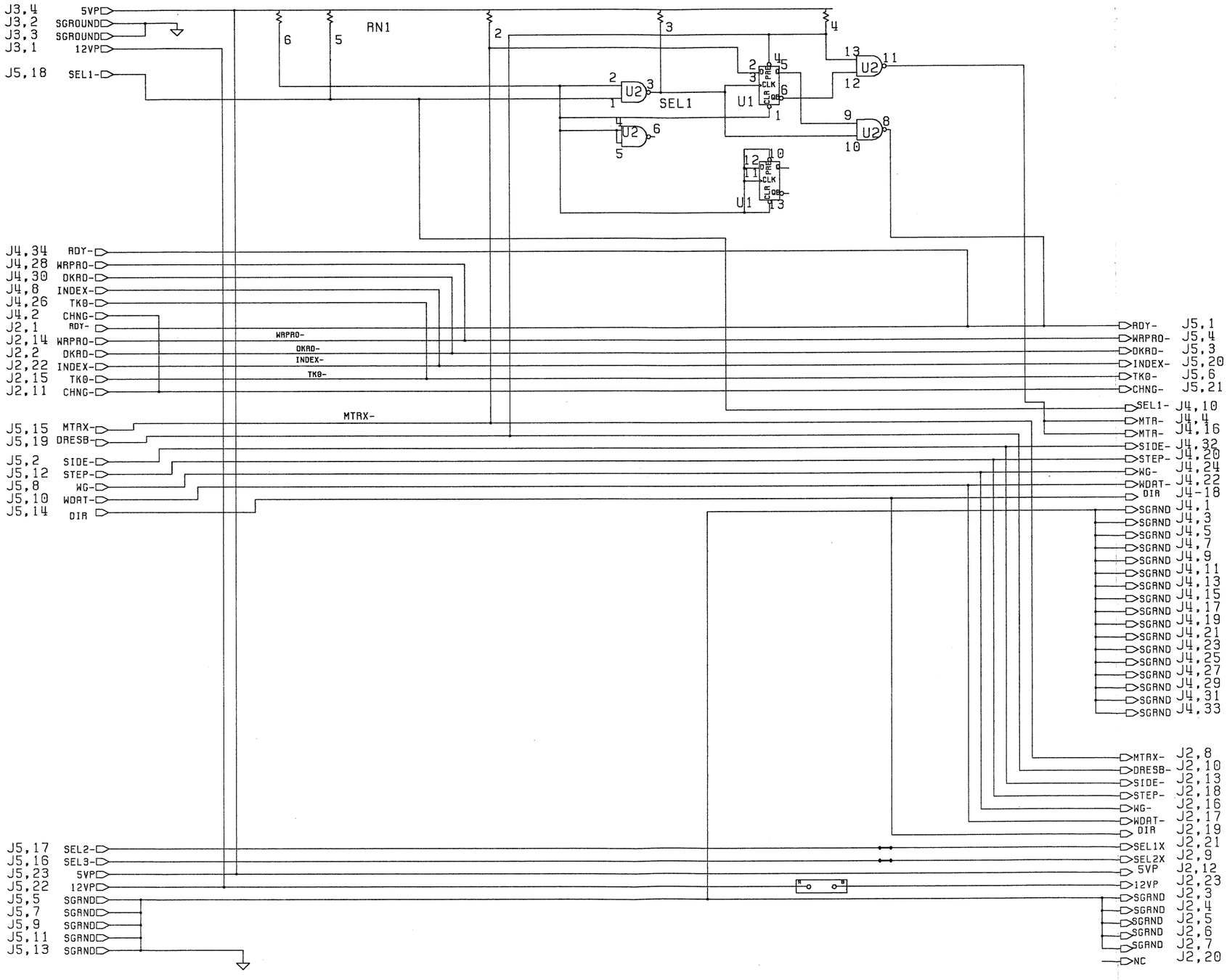
328016-01

RAM/ROM Daughter Board

SIZE D | D Needle 10-18-85 | REV 0.5

Drawn By LM Sinkovic | SHEET 1 OF 1

REVISION HISTORY			
REV	ECO NUMBER	DATE	BY :



WARNING:

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COMMODORE-AMIGA INC.
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328018-01

EXT3ICRD

EXTERNAL 3.5 DISC CONTROL PCB

SIZE		REV
D	S CRAIMER 08-04-85	1.2
Drawn By: LM Sinkovic	SHEET 1 OF 1	

REVISION HISTORY			
REV	ECO NUMBER	DATE	BY

J5,2 5VLOCC
J5,1 SGROUND
.1uF
C1
1K 3
1K 6
RN1 1K 2 1K 8
1K 4
U1 SEL1 74LS132
U2 74LS74
U3 7438
MTR
RDYQ
J3,18 SEL1-

J4,34 RDY-
J4,28 WRPRO-
J4,30 DKRD-
J4,8 INDEX-
J4,26 TK0-

J2,1 RDY-
J2,14 WRPRO-
J2,2 DKRD-
J2,22 INDEX-
J2,15 TK0-
J2,11 CHNG-

WRPRO-
DKRD-
INDEX-
TK0-

RDY- J3,1
WRPRO- J3,4
DKRD- J3,3
INDEX- J3,20
TK0- J3,6
CHNG- J3,21
MTR- J4,4
MTR- J4,16
SEL1- J4,10
NC2 J4,2,6,12,14

J3,15 MTRX-
J3,19 DRESB-
J3,2 SIDE-
J3,12 STEP-
J3,8 WG-
J3,10 WDAT-
J3,14 DIR

SIDE- J4,32
STEP- J4,20
WGE- J4,24
WDAT- J4,22
DIR J4,18
SGND J4,1
SGND J4,3
SGND J4,5
SGND J4,7
SGND J4,9
SGND J4,11
SGND J4,13
SGND J4,15
SGND J4,17
SGND J4,19
SGND J4,21
SGND J4,23
SGND J4,25
SGND J4,27
SGND J4,29
SGND J4,31
SGND J4,33

R1 1K
U1 74LS132
U3 7438
Q1 PST518B
U1 74LS132
U3 7438
.1uF
C2

J3,17 SEL2-
J3,16 SEL3-
J3,23 5VP
J3,22 12VP
J3,5 SGND
J3,7 SGND
J3,9 SGND
J3,11 SGND
J3,13 SGND

MTRX- J2,8
DRESB- J2,10
SIDE- J2,13
STEP- J2,18
WG- J2,16
WDAT- J2,17
DIR J2,19
SEL1X J2,21
SEL2X J2,9
5VP J2,12
12VP J2,23
SGND J2,3
SGND J2,4
SGND J2,5
SGND J2,6
SGND J2,7
NC J2,20

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COMMODORE-AMIGA INC.
983 UNIVERSITY AVE.#D
LOS GATOS, CA 95030

328019-01

EXT5ICRD

EXTERNAL 5.25 FDD SELECT PCB

SIZE D | S CRAIMER 04-06-86 | REV 1.3

Drawn By LM Sinkovic | SHEET 1 OF 1

BGINX IS NOW CONNECTED TO PIN 95 thru J5 ON J1

NOTE1: RN5 thru RN10 inclusive, are BOTH pullup AND pulldown.

NOTE2: All signals are common, Unless the signal name is to the LEFT of its respective J connector. For example BGACK* is a common signal while BG1* is NOT a common signal. Exceptions are J8 and J10.

LAST USED	NOT USED
C21	J6, J7
J10	RN2-4, -5, -6, -7, -10
RN10	RN3-9,-10
U16	RN4-7, -8, -9, -10
	U3 11,9
	U4 11,9
	U10 4,5,6;9,10,8;12,13,11
	U11 4,5,6;9,10,8;12,13,11

REVISION HISTORY			
REV	ECO NUMBER	DATE	BY

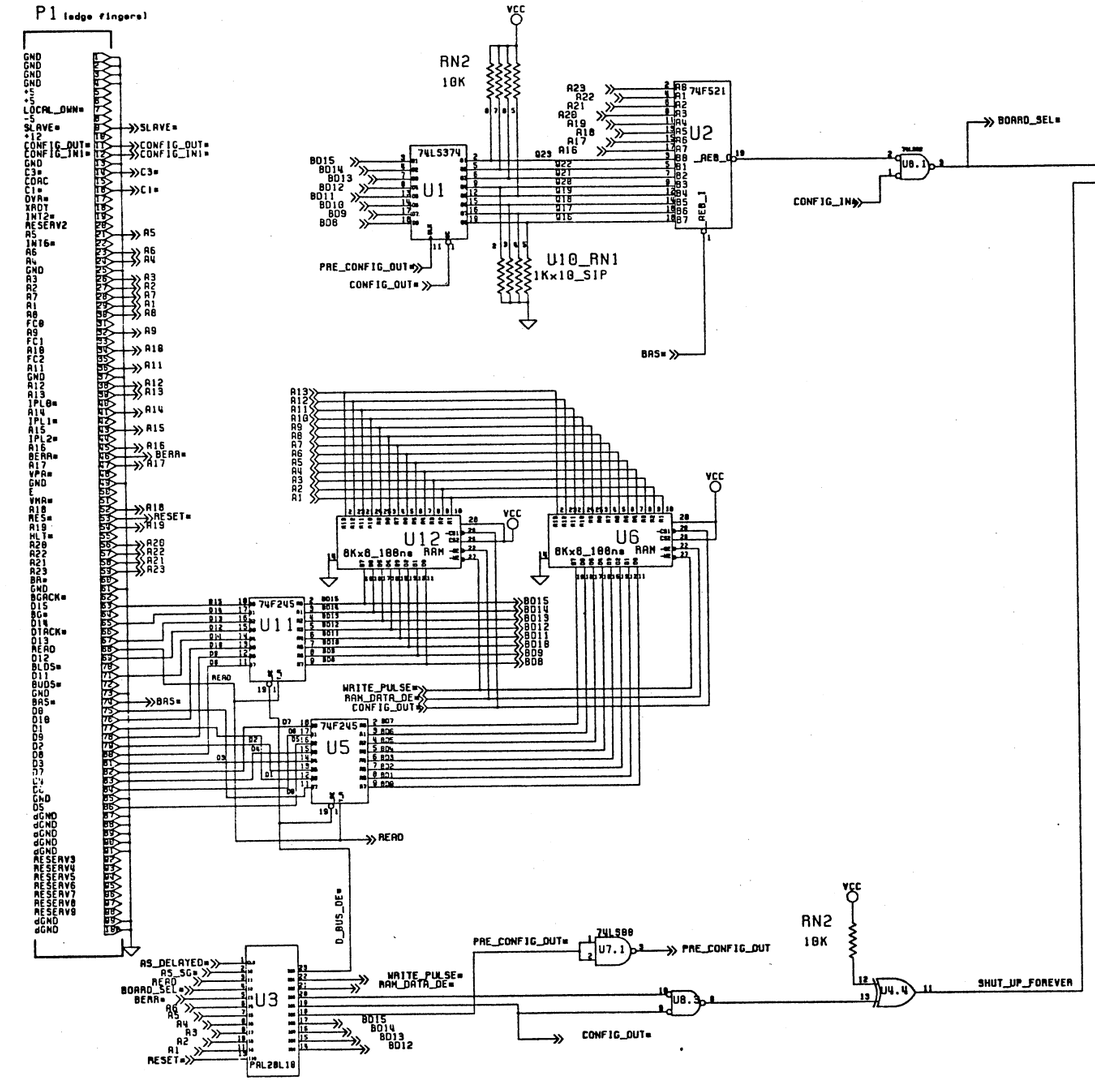
COMMODORE-AMIGA INC.
983 UNIVERSITY AVE. #D
LOS GATOS, CA 95030

328050-01

ZORRO Expansion

SIZE D | B Kolb | 04-04-88 | REV 1.9

Drawn by LM Sinkovic | SHEET 1 OF 1



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328060-01

Expansion Test RAM

SIZE D | B Kolb | 81-14-86 | REV 0.1

Drawn By LM Sinkovic | SHEET 1 OF 1