

A2232 MULTIPOINT SERIAL CARD FUNCTIONAL SPECIFICATION

DESCRIPTION

The A2232 Multipoint Serial Card is a standard 100 pin Zorro II expansion card for the Amiga 2000. It provides the Amiga with 7 additional standard RS232 serial ports, capable of speeds up to 19.2 kbaud. For more serial channels, additional A2232 boards can be plugged into the system at the same time.

SERIAL PORTS

All 7 of the serial ports are available at the rear of the board via 7 8-pin mini DIN connectors. The board comes with 7 short adapter cables which can be plugged into each of these connectors, which provides a more standard DB-25 connection.

signal	8 pin mini DIN	DB-25	dir
TxD / RxD	1	2	out/in
RxD / TxD	2	3	in/out
Request to Send (RTS)	3	4	out
Clear to Send (CTS)	4	5	in
Data Set Ready (DSR)	5	6	in
Signal Ground	6	7	
Data Carrier Detect (DCD)	7	8	in
Data Terminal Ready (DTR)	8	20	out

In order to simplify connections, the transmit data (TxD) and receive data (RxD) signals can be swapped on the A2232 board. There is an 8 jumper block (JB1) at the back of the board which makes this possible. Each of the 7 serial channels is associated with 4 possible jumper locations, and uses 2 of the jumpers. Figure 1 shows the schematic for this jumper block. Figure 2 shows how to configure the shorting blocks for a single channel.

All unused inputs have pullups on the board which keeps them at their 'TRUE' value if not connected. This greatly simplifies things if you are only using a 3-wire connection.

A2232 SYSTEM CONFIGURATION

The A2232 expansion card conforms to the auto-config protocol.

auto-config size	64k bytes
manufacturer code	202 (hex)
product number	46 (hex)

A block diagram of the board is shown in figure 3.

An 8 bit processor was incorporated in the A2232 in order to remove the burden of handling I/O from the Amiga system's main CPU. Also, since the Amiga is multi-tasking, it is impossible to ensure that the system's CPU can respond in a timely manner in order to service the needs of the I/O channels. The 8 bit processor used is a 65CE02, which is an **enhanced** version of the 6502, providing faster operation through new instructions and higher operating speeds.

The 6502 and the Amiga communicate mainly through the 16k bytes of shared RAM. The Amiga also has control over the 6502's *RESET and *IRQ signals. The 6502 can interrupt the Amiga via the *INT2 interrupt line. The Amiga must clear this interrupt itself.

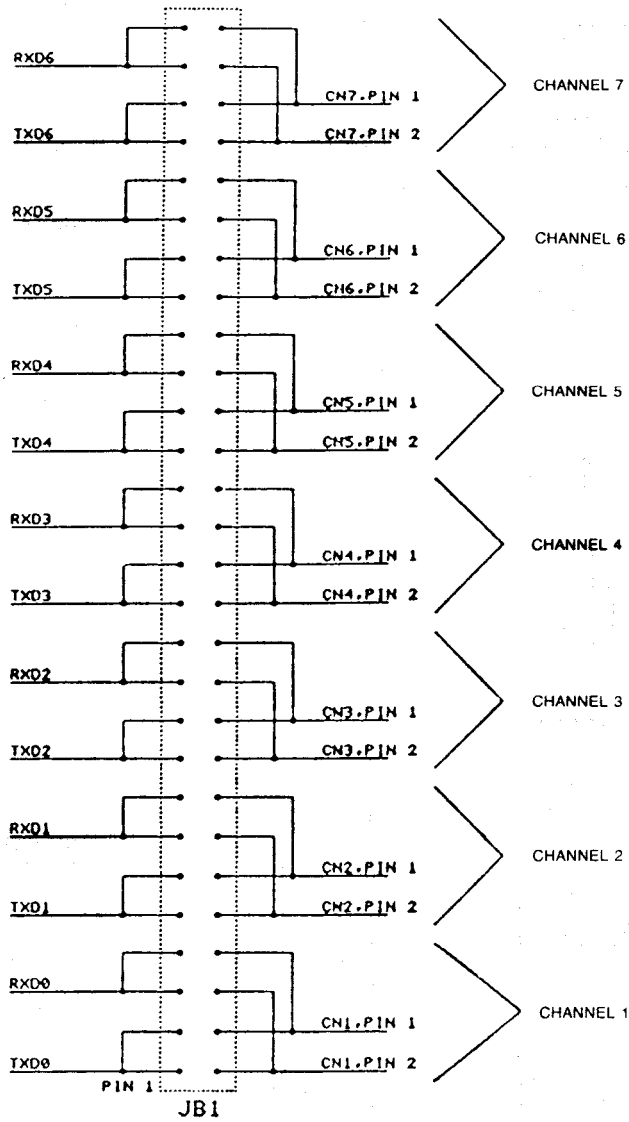


FIGURE 1 — JUMPER BLOCK SCHEMATIC

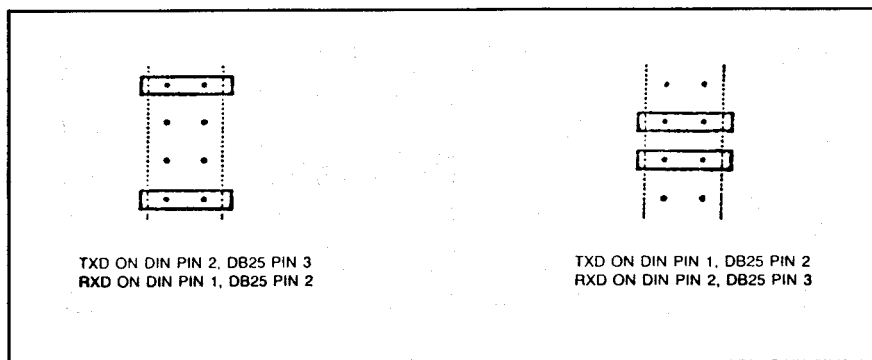


FIGURE 2 — OPTIONS FOR CONNECTING TXD & RXD FOR EACH CHANNEL

board offset	description
\$0000-\$3FFF	16k bytes of shared RAM
\$4000	reset the *INT2 interrupt caused by the 6502
\$8000	set 6502's *RESET line low
\$A000	set 6502's *IRQ line low
\$C000	set 6502's *RESET line high

AMIGA's MEMORY MAP OF A2232

The control signals listed above are affected when the Amiga does an access (read or write) to the locations listed. No information is passed over the data bus.

The 6502 executes code which is downloaded by the Amiga into shared RAM. When the Amiga goes through a hardware reset, the *RESET line to the 6502 is latched low, keeping it frozen. This gives the Amiga a chance to download the code which the 6502 is to execute. After the code is downloaded, the 6502 is started when the Amiga does a dummy access at board offset of \$C000, allowing the *RESET line to go high. The Amiga can freeze the 6502 at any time later by accessing location \$8000, latching the *RESET line low again. More or different code may now be loaded, and the 6502 restarted again.

The 6502 has control over all 7 of the 6502 ACIAs. The Amiga cannot access them directly.

address	description
\$0000-\$3FFF	16k bytes of shared RAM
\$4400	ACIA for channel 1
\$4C00	ACIA for channel 2
\$5400	ACIA for channel 3
\$5C00	ACIA for channel 4
\$6400	ACIA for channel 5
\$6C00	ACIA for channel 6
\$7000	set Amiga's *INT2 interrupt low
\$7400	ACIA for channel 7
\$7C00	8520 CIA
\$8000	Reset (set high) the *IRQ caused by the Amiga
\$C000-\$FFFF	16k bytes of shared RAM

6502's MEMORY MAP OF THE A2232

Note that 16k of RAM appears to the 6502 in 2 places. This was done so that the 6502's 'zero page' of memory and the reset vectors could be handled with the same RAM.

A2232 System Timing

The 7 Megahertz clock coming from the Amiga is used to drive a state machine that generates the clocks used on the A2232. The PH10 clock which drives the 6502 is divided down from the 7M clock. Normally, the 6502 runs at 3.5 Mhz. However, so that the board can use the less expensive 2 Mhz 6551's, the 6502 must slow down to 1.75 Mhz when accessing the ACIA's (6551's). Since the 6551's are provided with a constant 1.75 Mhz clock, the 6502 must first sync up with the 6551's clock before completing the access. The 6502 is also slowed down while the Amiga accesses the shared RAM. This is done by keeping the PH10 clock low while the 68000 accesses the RAM, effectively halting the 6502.

Figure 4 illustrates the operation of the state machine. Each of the states is 1 7M cycle long (140 nanoseconds). The arrows connecting each of the states are numbered as different transitions.

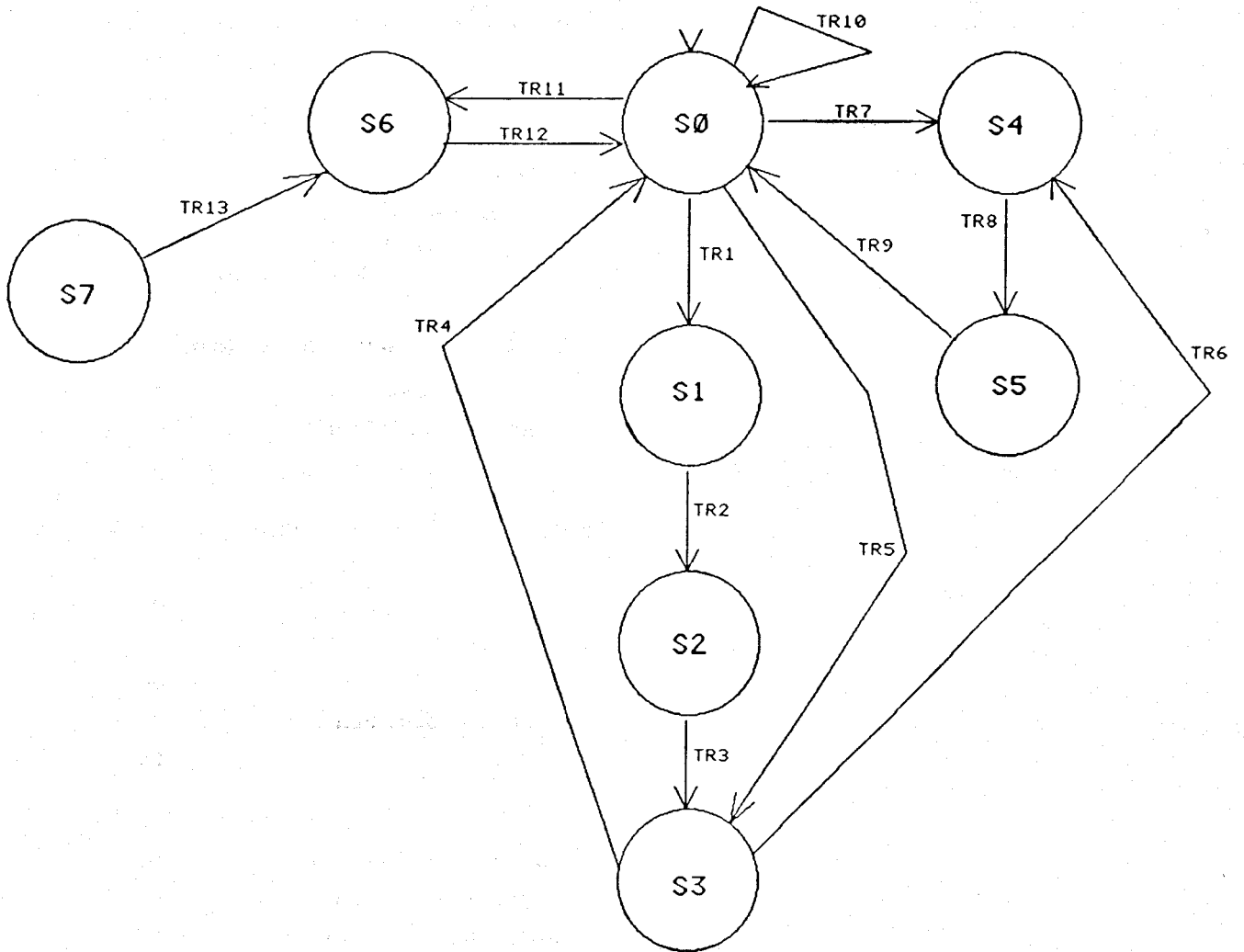


FIGURE 4 — A2232 STATE MACHINE DIAGRAM

6502 RAM ACCESS

The 6502 accesses ram during states S0 and S3. If it is determined during S0 that the 6502 wants to access the RAM, TR5 is used, bypassing S1-S2. The Phi0 clock is low during S0, and goes high during S3, yielding the 3.5 Mhz clock. At the end of S3, there are 2 different transitions that can be taken. TR4 is taken if the 68000 is not waiting to access the RAM. If the 68000 is waiting to get at the RAM, but is not properly synched with the C1 clock, TR4 is also taken. TR6 is taken when the 68000 is waiting, and is properly synched.

Referring to figure 5 ...

(7)	read data setup time : ≥ 40 nsecs
280	Phi2 cycle time
- 50	6502 address setup time (max)
- 15	74F257 delay (max)
- 15	*CS goes low, 20L8B delay (max)
- 100	RAM access time
- 18	74LS245 delay (max)
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82	

(8)	read data hold time : ≥ 10 nsecs
5	20L8B delay (min)
+ 5	74LS245 turn off time (min)
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10	

(10)	write data setup time : ≥ 50 nsecs
140	Phi2 high time
- 50	6502 write data delay (max)
- 18	74LS245 delay (max)
- 30	Phi0 to Phi2 delay (max)
+ 5	20L8B PAL delay (min)
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47	

(11)	write data hold time : ≥ 5 nsecs
5	Phi0 to Phi2 delay (min)
+ 5	20L8 PAL delay (min)
+ 5	74LS245 turn off (min)
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15	

6502 ACCESSING 6551's

Since the 6551's can only run at 1.75 Mhz, they must be provided with a constant 1.75 Mhz (or less) clock. In order for the 6502 to access the 6551, it must slow down to this speed as well. During S0, the state machine determines that the 6502 wants to access a 6551. If the clock driving the 6551 is currently low, then the 6502 is in sync with the 6551 (the PH10 clock is always low during S0). TR1 is taken and the access may continue. If the 6551 clock is high, then they are out of sync, and TR11 is taken. TR12 immediately follows TR11, during which the 6551 clock is inverted. The state machine now determines during S0 that they are in sync, and TR1 can be taken. PH10 and the 6551 clock are both low during S1, and go high during S2 and S3, yielding 1.75 Mhz. At the end of S3 the same decisions as described at the end of a RAM access are again executed.

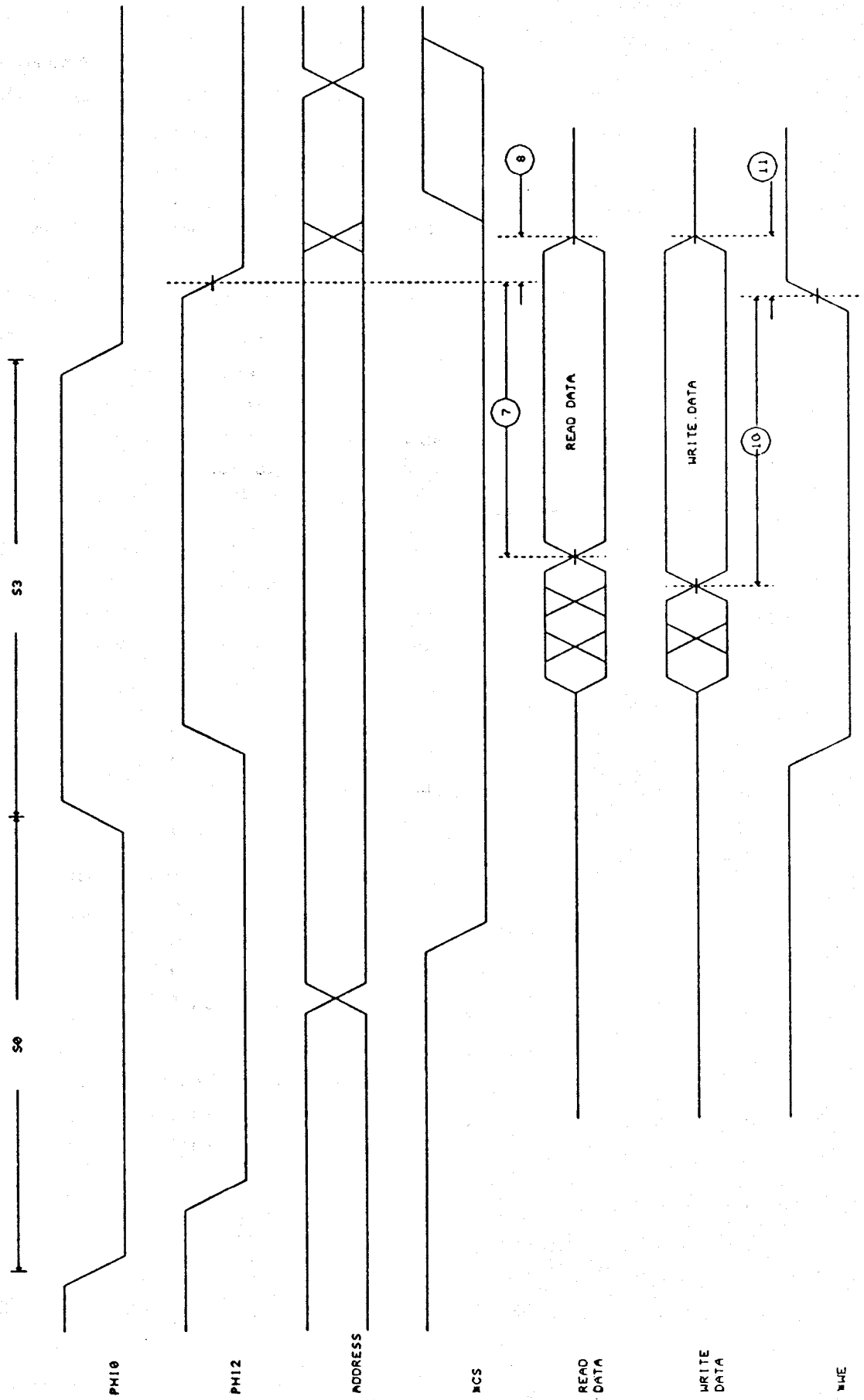


FIGURE 5 — 6502 RAM ACCESS

Referring to figure 6 ...

- (1) setup time for ADR, RSO-3,R/W,CS,*CS : ≥ 70 nsecs

The latest of these signals is *CS.

280	6551 CLK low time
- 30	Phi0 to Phi2 delay (max)
- 40	6502 Address setup time (max)
- 30	74LS138 delay (max)
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180	

- (2) write data setup time : ≥ 60 nsecs

280	6551 CLK high time
- 30	Phi0 to Phi2 delay (max)
- 50	6502 write data setup time (max)
- 18	74LS245 delay (max)
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182	

- (3) write data hold time : ≥ 20 ns

5	Phi0 to Phi2 delay (min)
+ 5	20L8B delay (min)
+ 5	74LS245 turn off time (min)
<hr/>	
15	(case 1)
5	Phi0 to Phi2 delay (min)
+ 5	6502 write data hold (tHD min)
+ 5	74LS245 in to out delay (min)
<hr/>	
15	(case 2)

- (4) read data setup time : ≥ 40 nsecs

280	Phi2 high time
+ 5	Phi0 to Phi2 delay (min)
- 150	read data access of 6551 (max)
- 18	74LS245 delay (max)
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107	

- (5) read data hold time : ≥ 10 nsecs

5	20L8B delay (min)
+ 5	74LS245 turn off time (min)
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10	

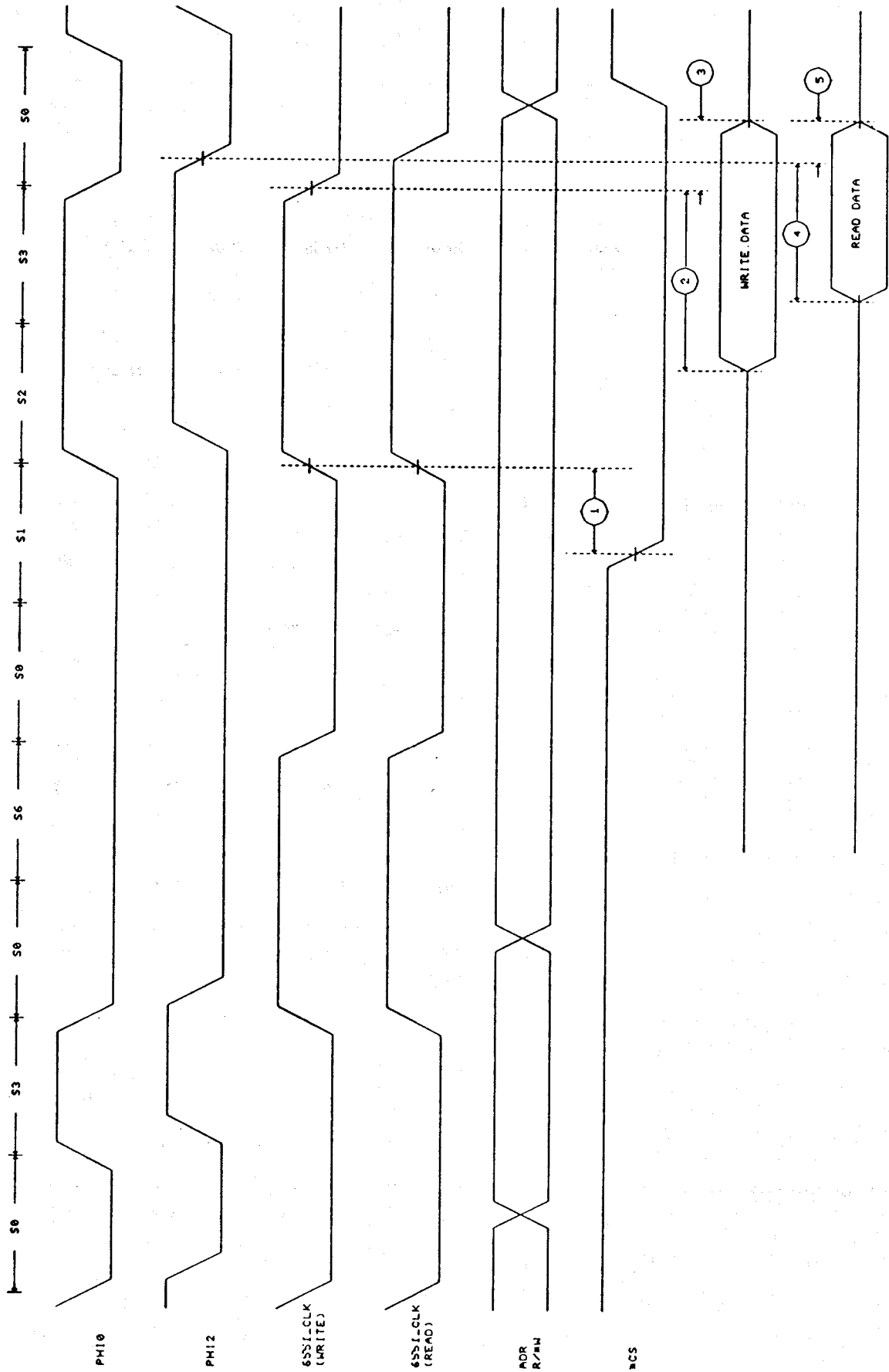


FIGURE 6 — ACCESSING 6551's

68000 RAM ACCESS

There are 2 states during which a 68000 request can be recognized. One of these is S3, which has already been described. During S0 a 68000 request can also be recognized. In both instances, the 68000 takes precedence. If the 68000 doesn't want access, then the 6502 is allowed to continue. During 68000 accesses the 6502 is halted by holding the Phi0 clock low. TR7 and TR6 both bring the state machine to S4, where the 68000 access is allowed to finish. From the time that the board is selected, it drives the override (*OVR) and *DTACK signals until the end of S5. As long as it may take for the state machine to get to S4, wait states are inserted into the 68000 access by keeping *DTACK high. At the beginning of S4 *DTACK goes low signalling to the 68000 that the access may be completed.

Referring to figure 7 ...

(15) read data setup time : ≥ 10 nsecs

referenced from the start of 68000 T4 ...

210	time from start of T4 to end of T6
- 15	Q delay of 16R8A PAL, Phi0 goes low (max)
- 30	Phi0 to Phi2 delay (max)
- 15	20L8B PAL delay, MUX goes low (max) (*RAMCS goes low too)
- 15	74F257 switching delay (max)
-100	RAM access time
- 10	74ALS245 delay (max)
- 18	74LS245 delay, on expansion bus (max)
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7	

(16) read data hold time : ≥ 0

Obvious.

(17) write data setup time : ≥ 50 nsecs

Assume that C3 transitions coincident with the rising edge of the 7M clock. Referenced from the rising C3 at the beginning of T4, the RAM *WE goes high 140 ns later. Referenced from the same rising edge of C3, the data becomes valid:

15	Q delay of 16R8A PAL (max)
+ 35	20L8 PAL delay (max)
+ 7	74F32 delay (max)
+ 20	74ALS245 turn on time (max)
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77 ns	

So, $140 - 74 = 66$ ns

(18) write data hold time : ≥ 5 nsecs

The write pulse went away half way through S5. The data and addresses stay valid through the rest of S5, or approximately 70 nsecs.

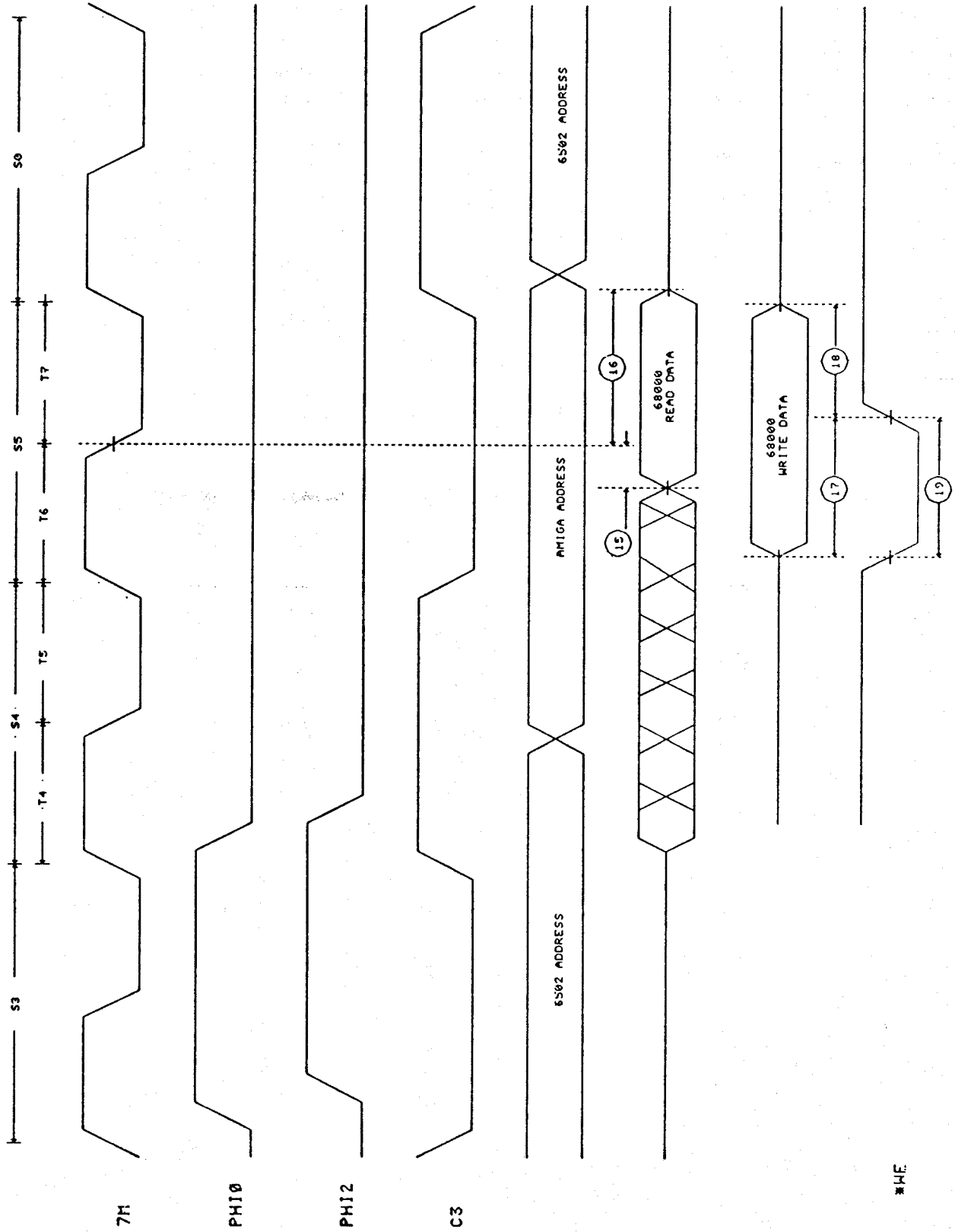


FIGURE 7 -- 68000 RAM ACCESS

Commodore International Spare Parts List

SHIPPING ASSEMBLIES

Commodore part numbers are provided for reference only and do not indicate the availability of spare parts from Commodore. Industry standard parts (Resistors, Capacitors, Connectors) should be secured locally. Part number information may vary according to country, some parts may not be available in all countries.

312859-01	A2232 SHIPPING ASSY (U.S.)	312859-03	A2232 SHIPPING ASSY (CANADA)
363128-01	BOX PACKING	363128-01	BOX PACKING
363127-01	BOX BULK SHIPPING	363127-01	BOX BULK SHIPPING
363100-01	MANUAL, USERS (SUB)	363100-01	MANUAL, USERS (SUB)
363375-01	MANUAL, USERS EFIGS	363375-01	MANUAL, USERS EFIGS
314877-04	BOOKLET SERVICE CENTER LIST	312864-02	CABLE ASSY MINI DIN TO DB25 (QTY = 7)
312864-02	CABLE ASSY MINI DIN TO DB25 (QTY = 7)	318882-01	CARD WARRANTY CANADA
318290-01	CARD WARRANTY U.S.	318928-01	BAG ANTI STATIC
318928-01	BAG ANTI STATIC	318896-01	S/W LICENSE AGREEMENT
318896-01	S/W LICENSE AGREEMENT	317769-01	DISKETTE ASSY
317769-01	DISKETTE ASSY	318940-01	SPACER CARDBOARD
318940-01	SPACER CARDBOARD	312860-01	PCB ASSY
312860-01	PCB ASSY	318733-02	MANUAL AMIGATERM
318733-02	MANUAL AMIGATERM	318556-02	CARD DISK EXCHANGE CANADA
312341-02	CARD DISK EXCHANGE		
312859-02	A2232 SHIPPING ASSY (EFIGS)	312859-04	A2232 SHIPPING ASSY (AUSTRALIA)
363128-01	BOX PACKING	363128-01	BOX PACKING
363127-01	BOX BULK SHIPPING	363127-01	BOX BULK SHIPPING
363100-01	MANUAL, USERS (SUB)	363100-01	MANUAL, USERS (SUB)
363375-01	MANUAL, USERS EFIGS	363375-01	MANUAL, USERS EFIGS
312864-02	CABLE ASSY MINI DIN TO DB25 (QTY = 7) (CAN SUB to -01)	312864-02	CABLE ASSY MINI DIN TO DB25 (QTY = 7)
318928-01	BAG ANTI STATIC	318884-01	CARD WARRANTY AUSTRALIA
317769-01	DISKETTE ASSY	318928-01	BAG ANTI STATIC
318940-01	SPACER CARDBOARD	317769-01	DISKETTE ASSY
312860-01	PCB ASSY	318940-01	SPACER CARDBOARD
318733-02	MANUAL AMIGATERM	312860-01	PCB ASSY
		318733-02	MANUAL AMIGATERM

Commodore International Spare Parts List

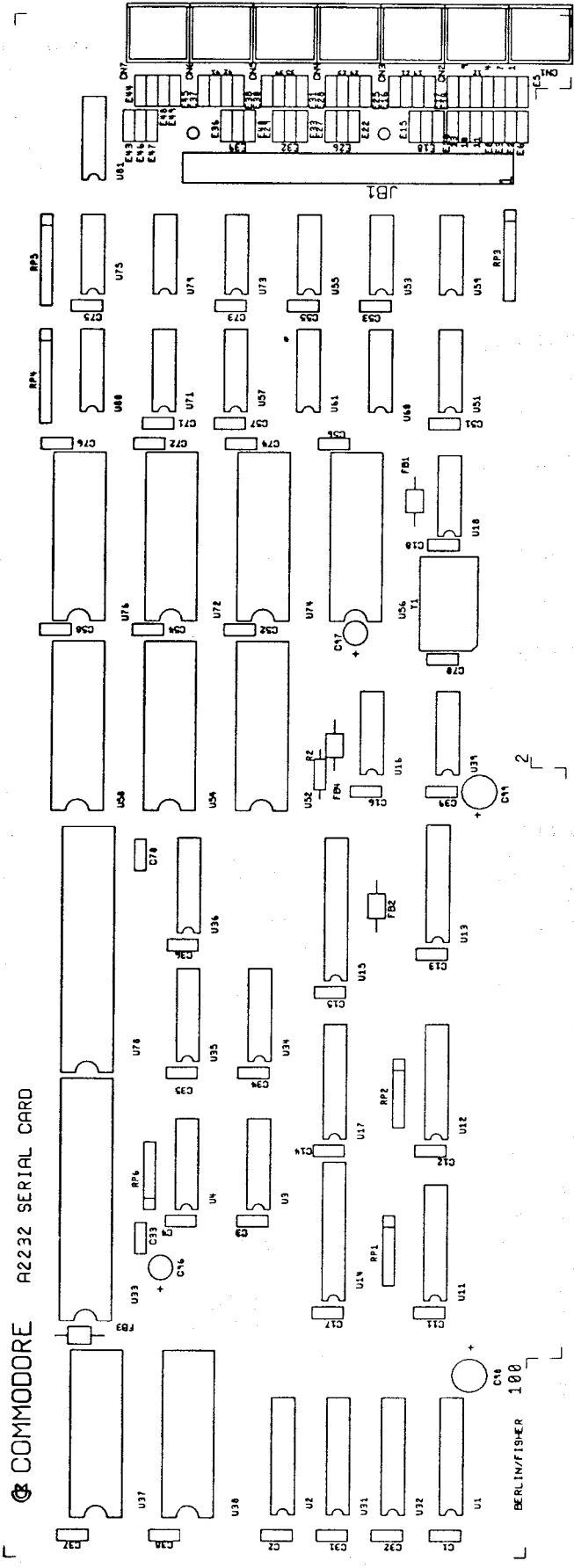
PCB Components

PCB Assembly #311611-01

Commodore part numbers are provided for reference only and do not indicate the availability of spare parts from Commodore. Industry standard parts (Resistors, Capacitors, Connectors) should be secured locally. Part number information may vary according to country, some parts may not be available in all countries.

IC COMPONENTS			RESISTORS		
312860-01	PCB ASSY A2232 SERIAL CARD		902441-22	PAK 6 PIN SIP 1K	RP1,RP6
318029-03	8520A-1	U78	902441-31	PAK 6 PIN SIP 4.7K	RP2
390373-01	16R8A PAL	U13	902442-55	PAK 8 PIN SIP 4.7K	RP3-RP5
390370-02	16L8 PAL	U17	901550-01	1K 5% 1/4 WATT	R2
390371-02	20L8A PAL	U15	901550-18	2.2K 5% 1/4 WATT	R3,R4
390372-03	20L8B PAL	U14	CAPACITORS		
901521-06	74LS74	U18	900020-01	.1 UF - 50V 20%	C1-C4,C11-C18,C31-C39,
901522-30	7407	U39	390101-05	ELECT ALUM RAD LEAD 4.7 UF	C51-C58,C70-C76,C78
390077-01	74F32	U16	MISCELLANEOUS		
318041-01	74F521	U12	325566-16	OSCILLATOR 1.8432 MHZ	Y1
901521-16	74LS138	U36	251842-04	EMI FILTER 470PF	EMI 1-EMI 49
901521-46	74LS245	U31,U32	903025-01	FERRITE BEAD	FB1-FB4
390091-01	74F257	U3,U4,U34,U35	903345-29	CONN 56 PIN DIL HEADER .10 CENTERS	JB1
901521-29	74LS373	U11	390043-01	SHUNT FEMALE 2 POS	
318092-01	74ALS245	U1,U2	390218-02	CONN 8 PIN MINI DIN RECEPTACLE	CN1-CN7
901882-01	MC1488 QUAD DRIVER	U59-U61,U79-U81	312865-01	EXTENSION CARD PANEL	
901883-01	MC1489 QUAD RECEIVER	U51,U53,U55,U57,U71, U73,U75	906800-05	SCREW 3M X 6 LG PAN HEAD PHILLIPS - QTY 2	
901895-03	6551A UART	U52,U54,U56,U58,U72, U74,U76	316914-01	LABEL FCC ID A2232	
310024-02	8K X 8 SRAM 100 NS	U37,U38			
390375-02	LSI CPU 65CE02	U33			
901895-02	6551A UART	SUB FOR ITEM 21			
SOCKETS					
904150-08	20 PIN DIP	U13,U17			
390060-01	24 PIN DIP SOCKET	U14,U15			
904150-05	28 PIN DIP	U52,U54,U56,U58,U72, U74,U76			
904150-06	40 PIN DIP	U33,U78			

COMMODORE A2232 SERIAL CARD

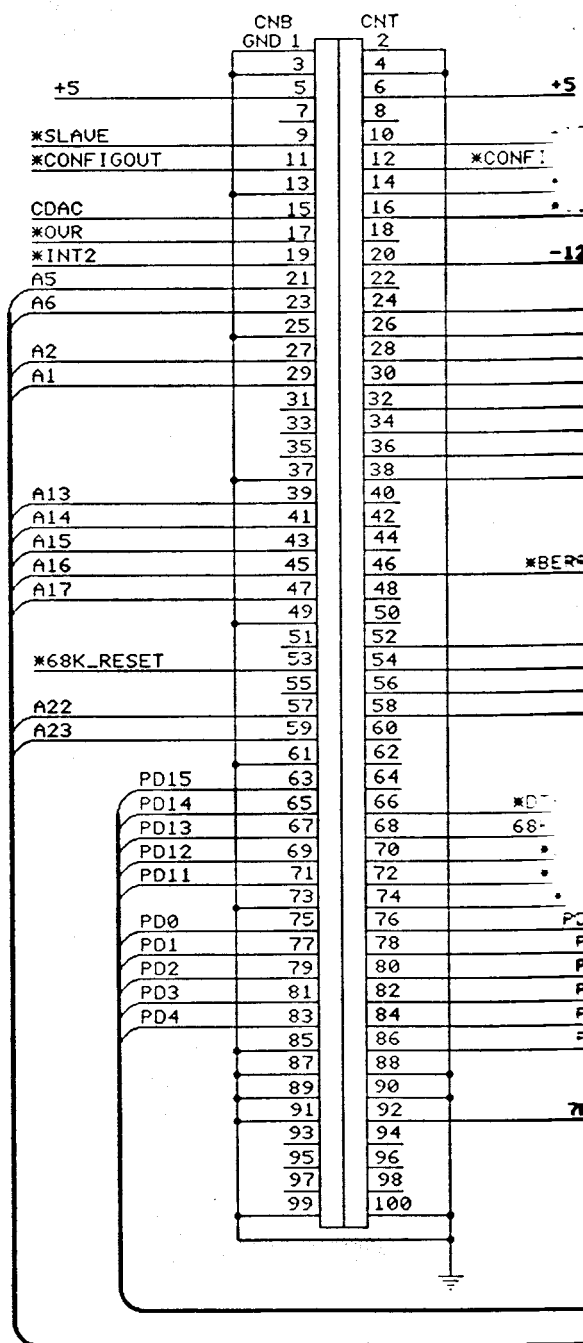


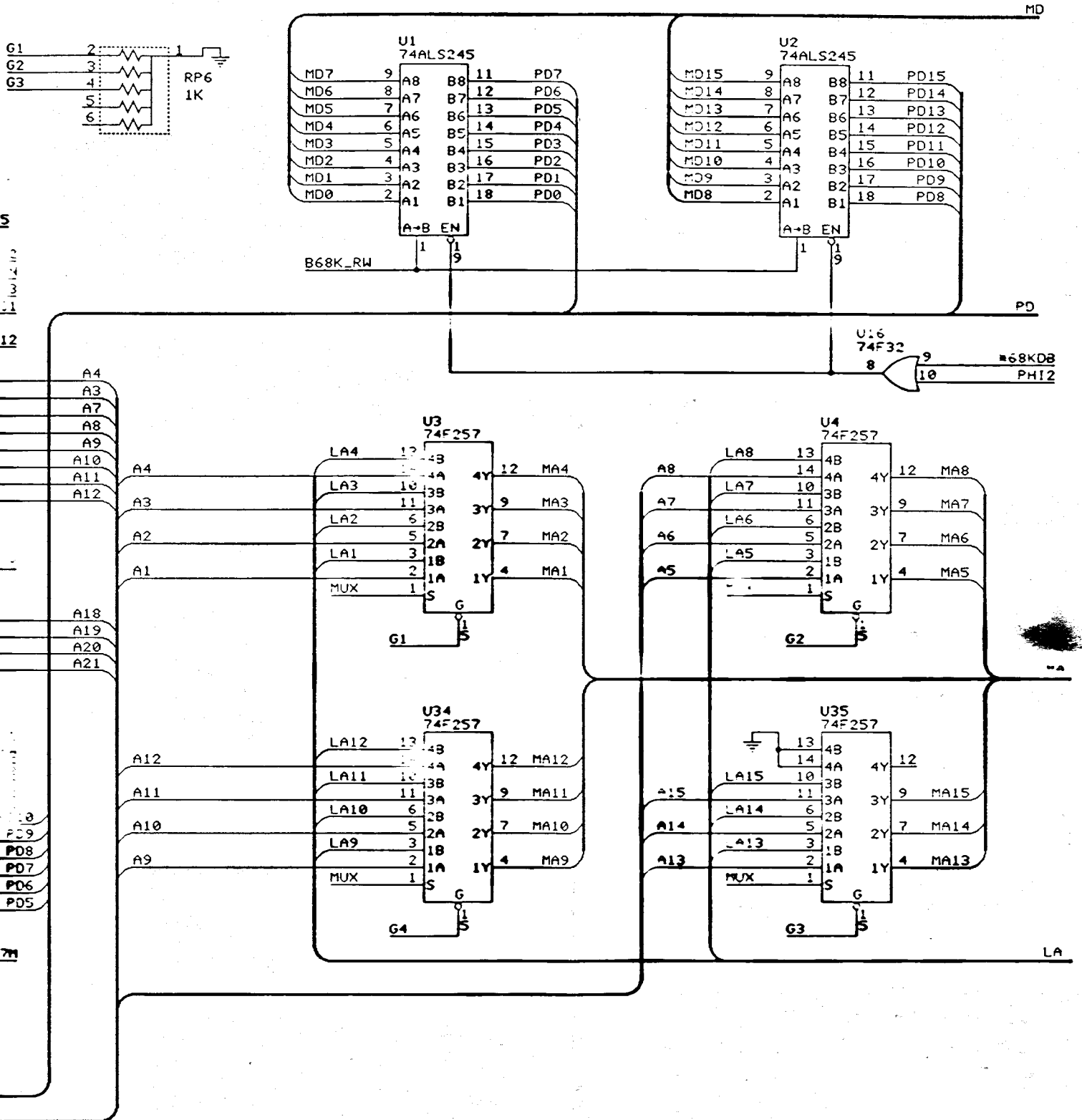
PCB BOARD LAYOUT #312863, REV. 5

A2232 SCHEMATIC #312861, REV. A — SCHEMATIC PAGE INDEX
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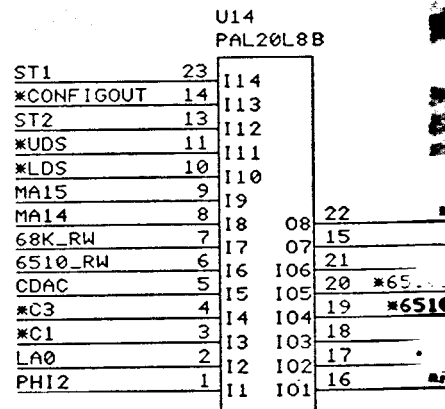
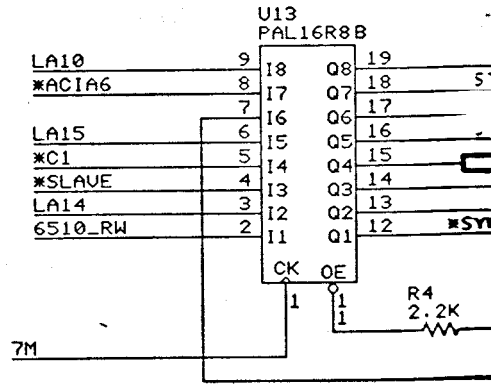
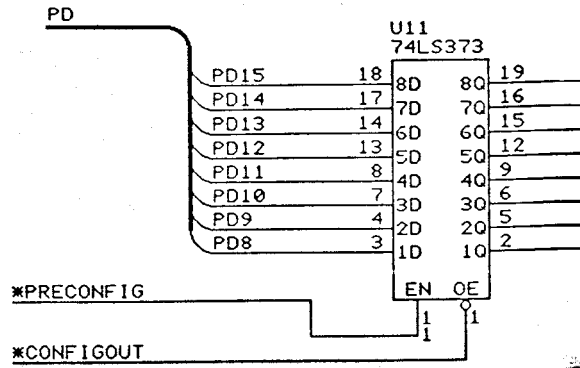
TITLE	SHEET	PAGE
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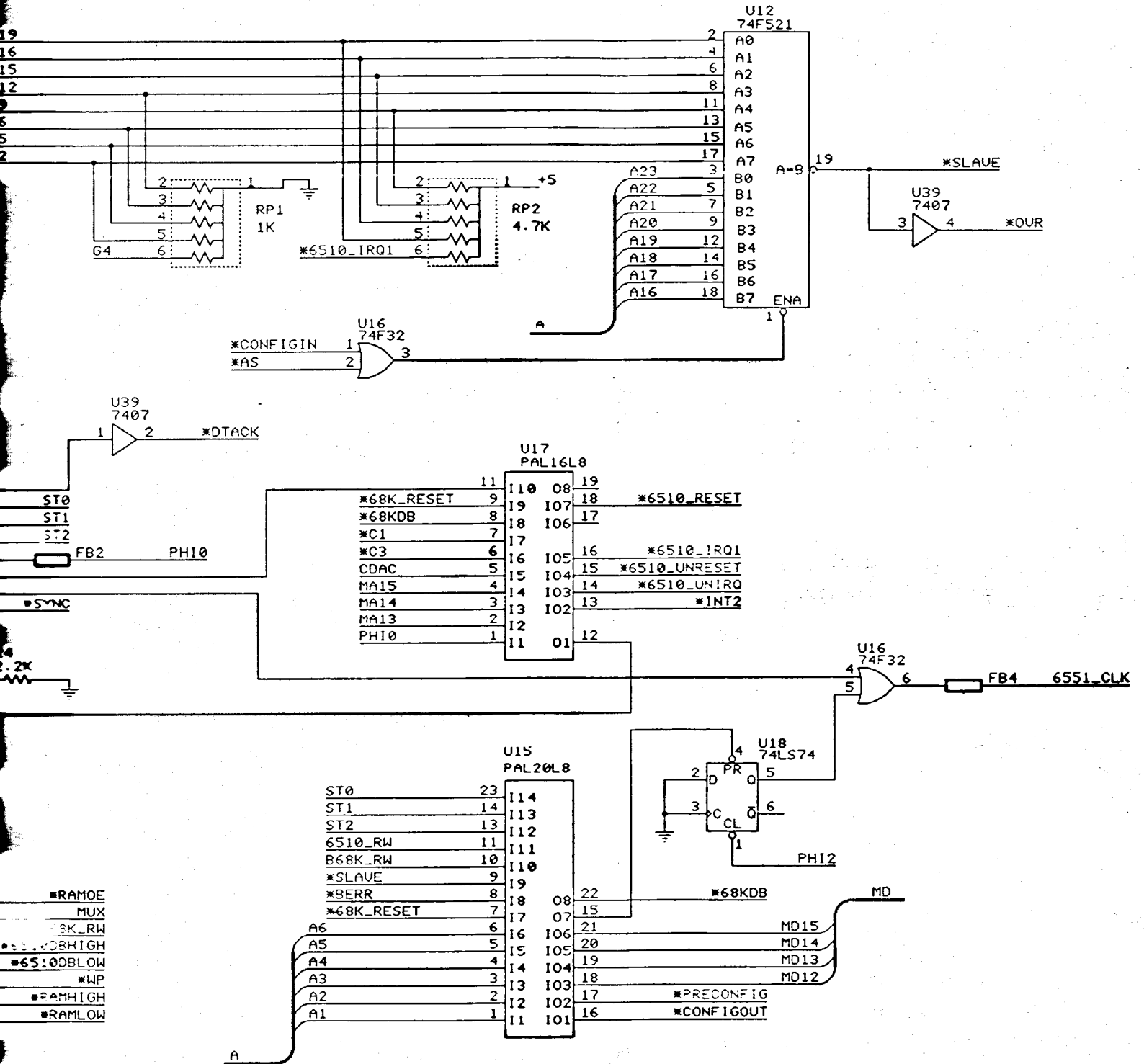
100 PIN
 EDGE CARD CONNECTOR



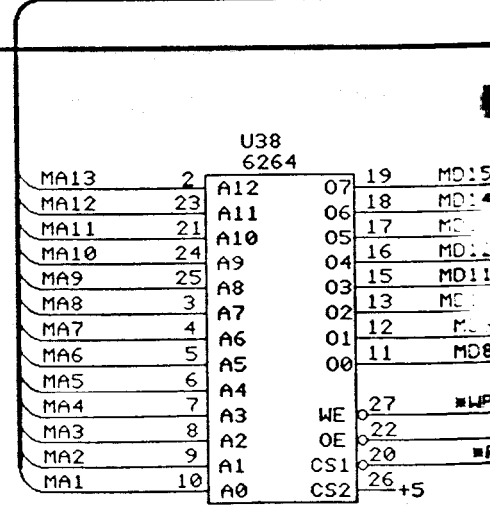
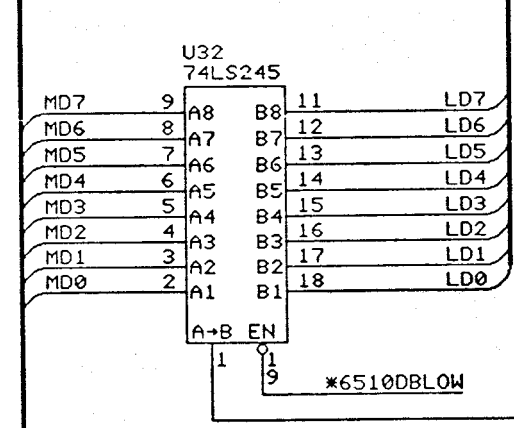
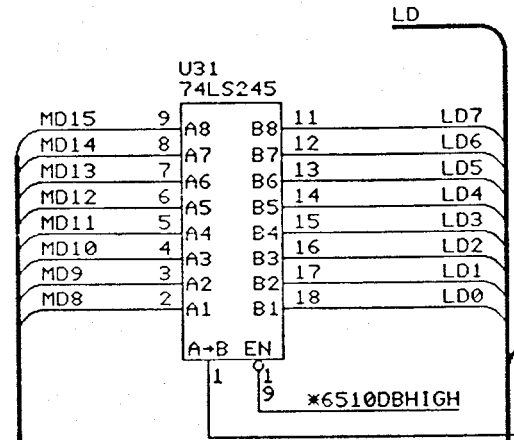


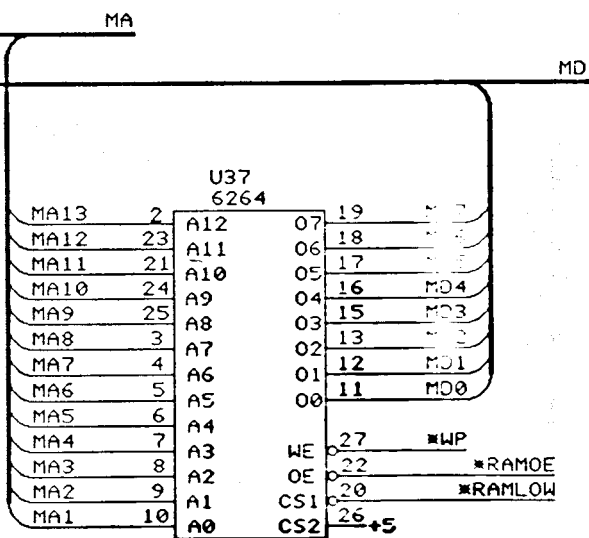
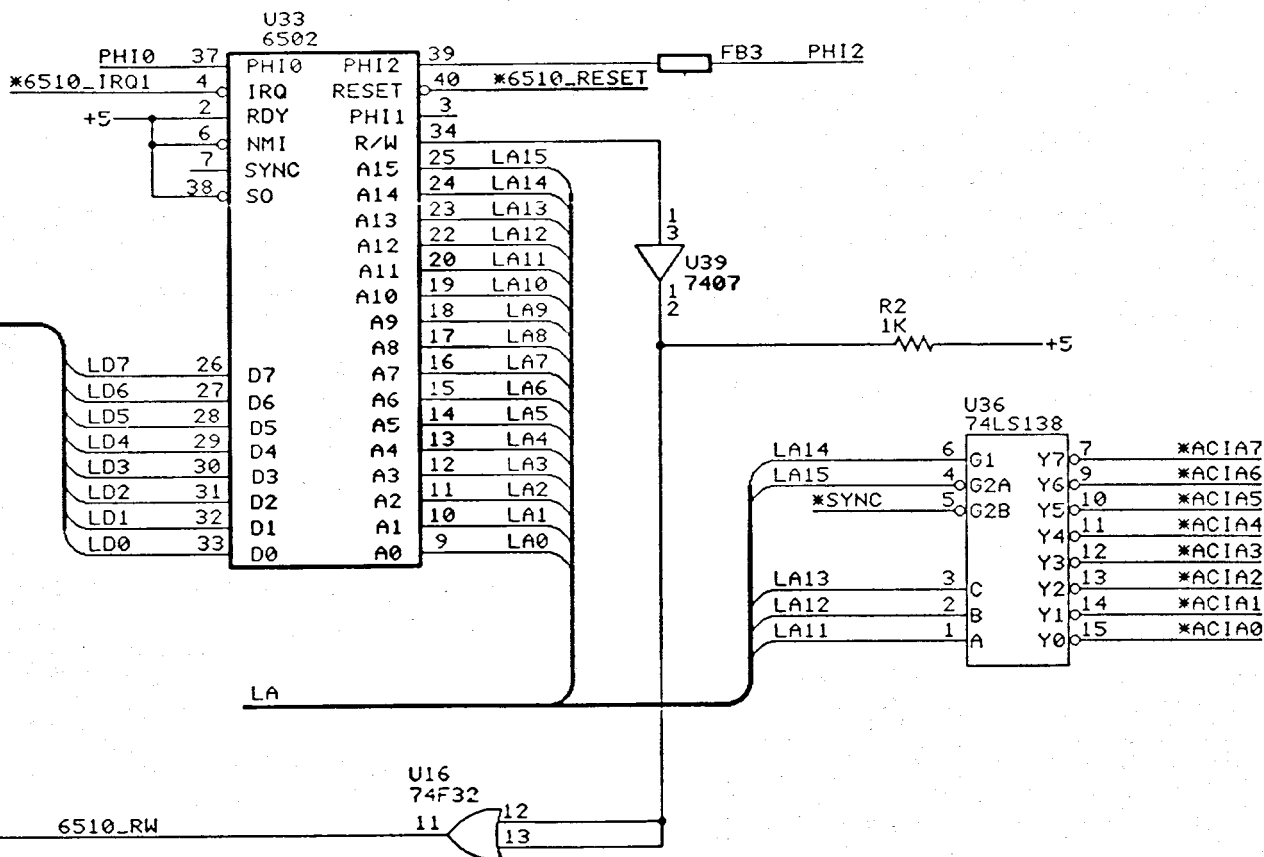
Schematic #312861, Rev. A
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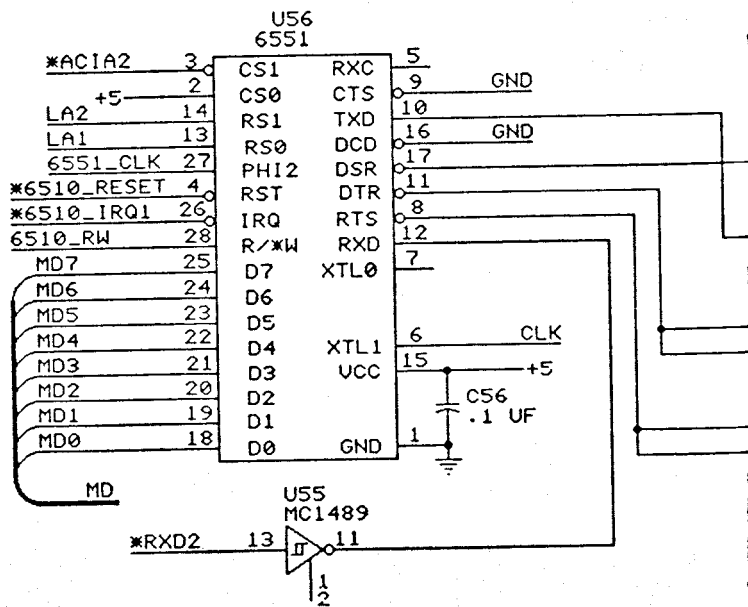
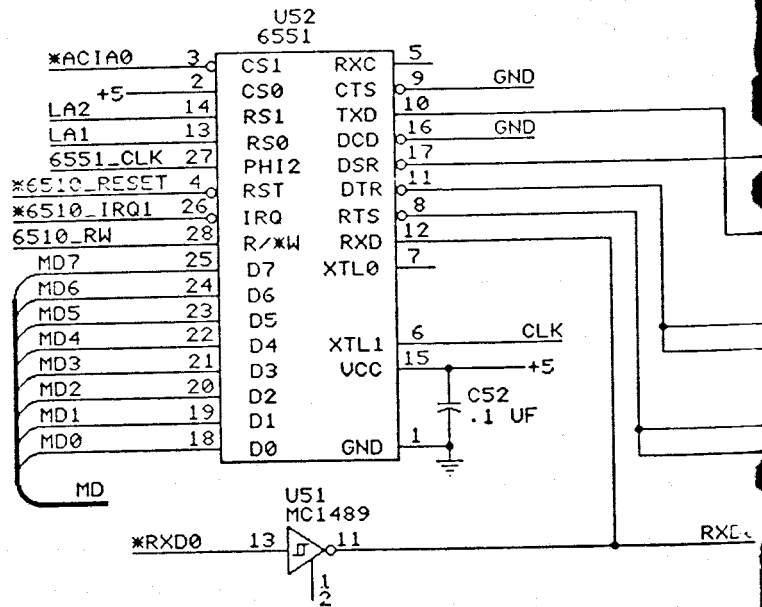


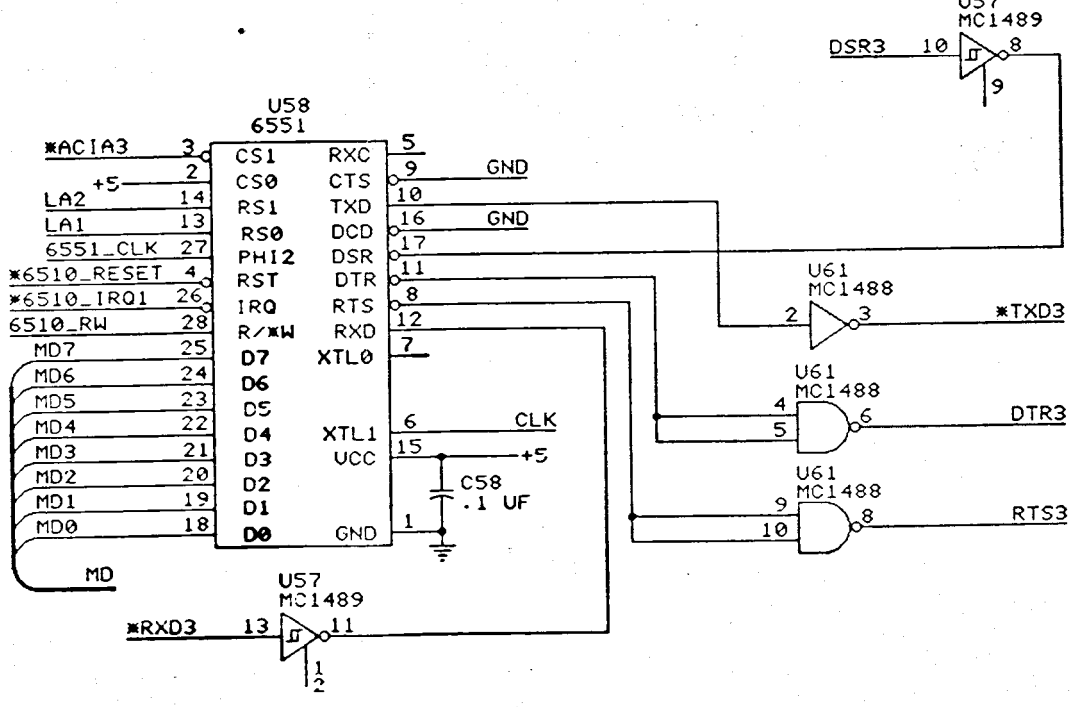
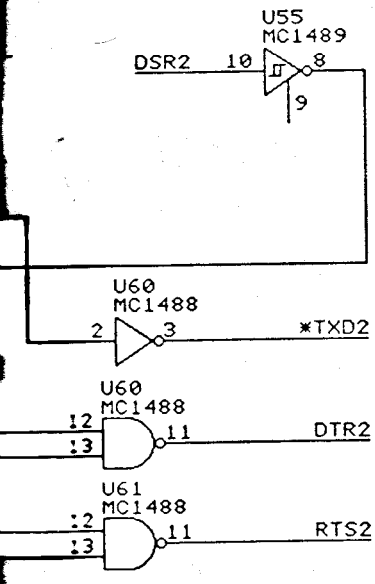
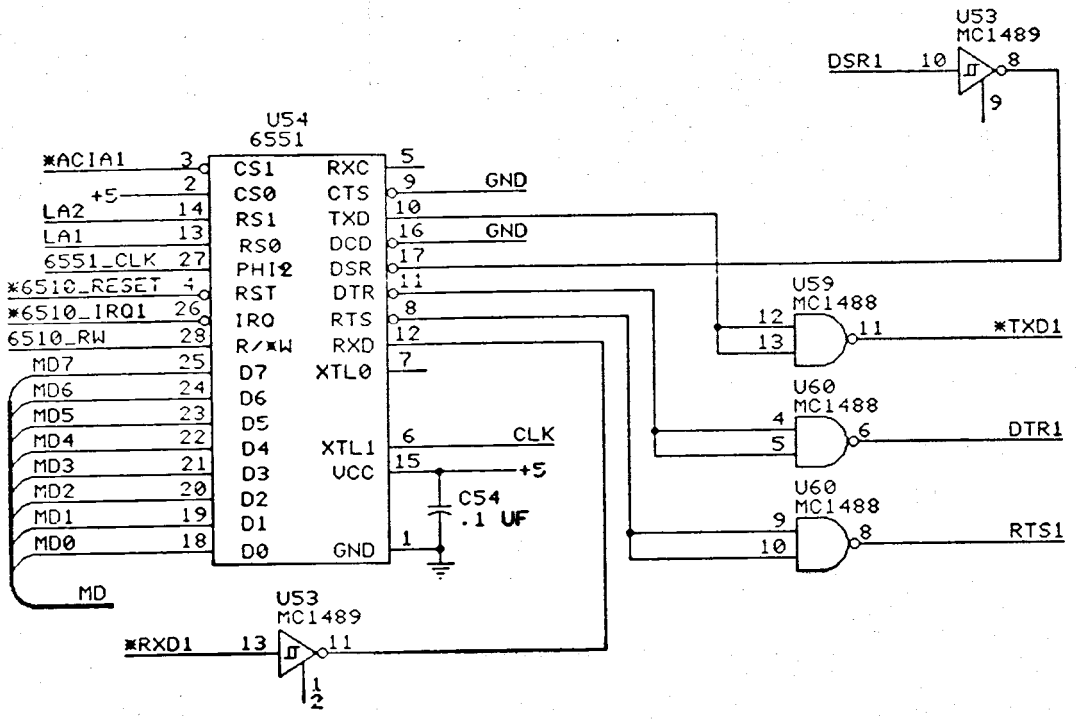
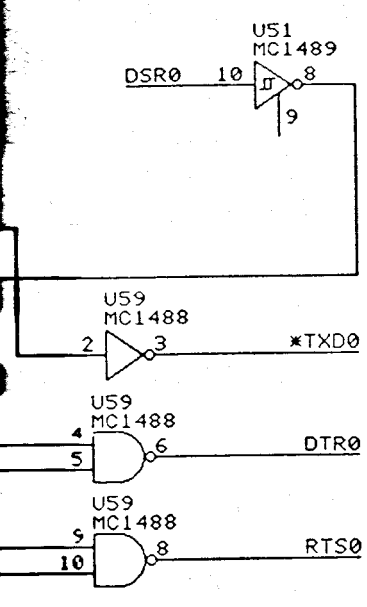
Schematic #312861, Rev. A
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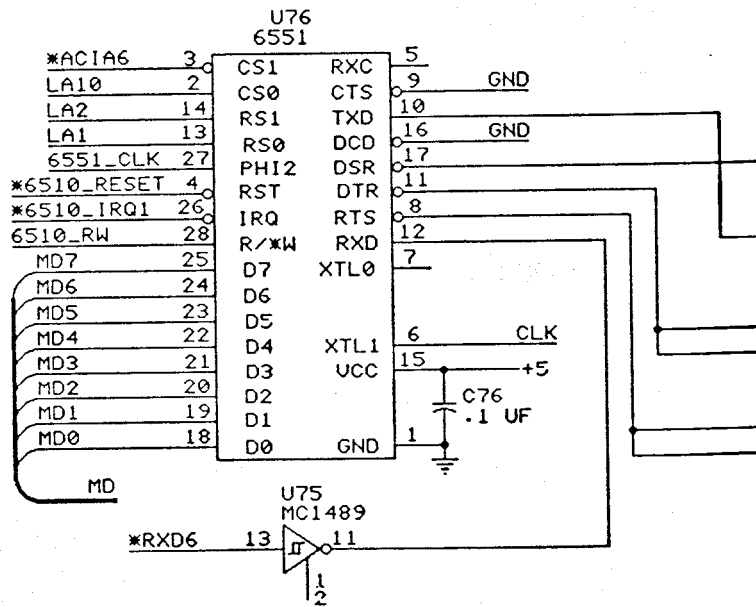
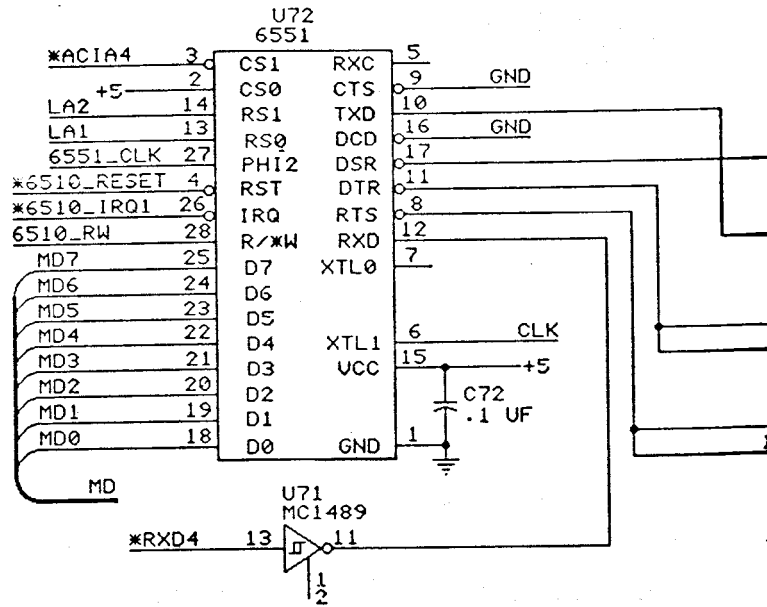


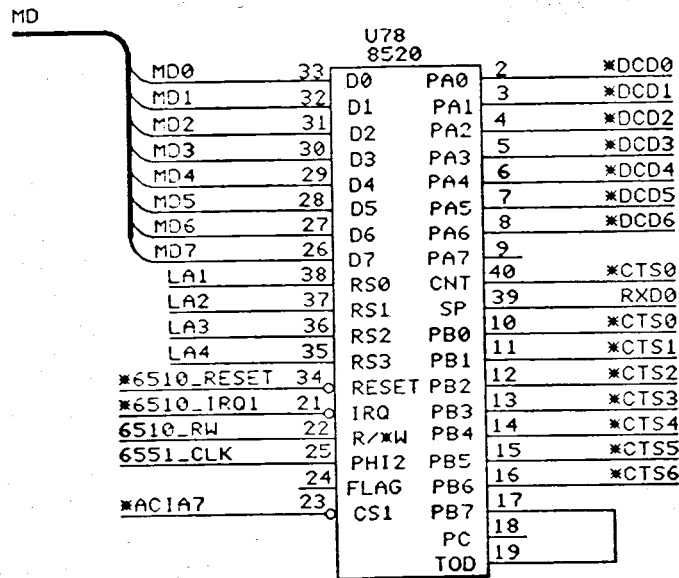
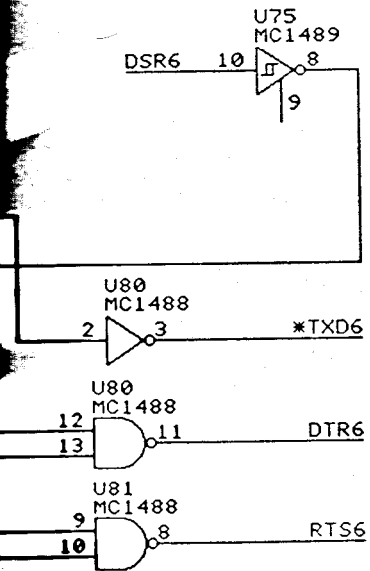
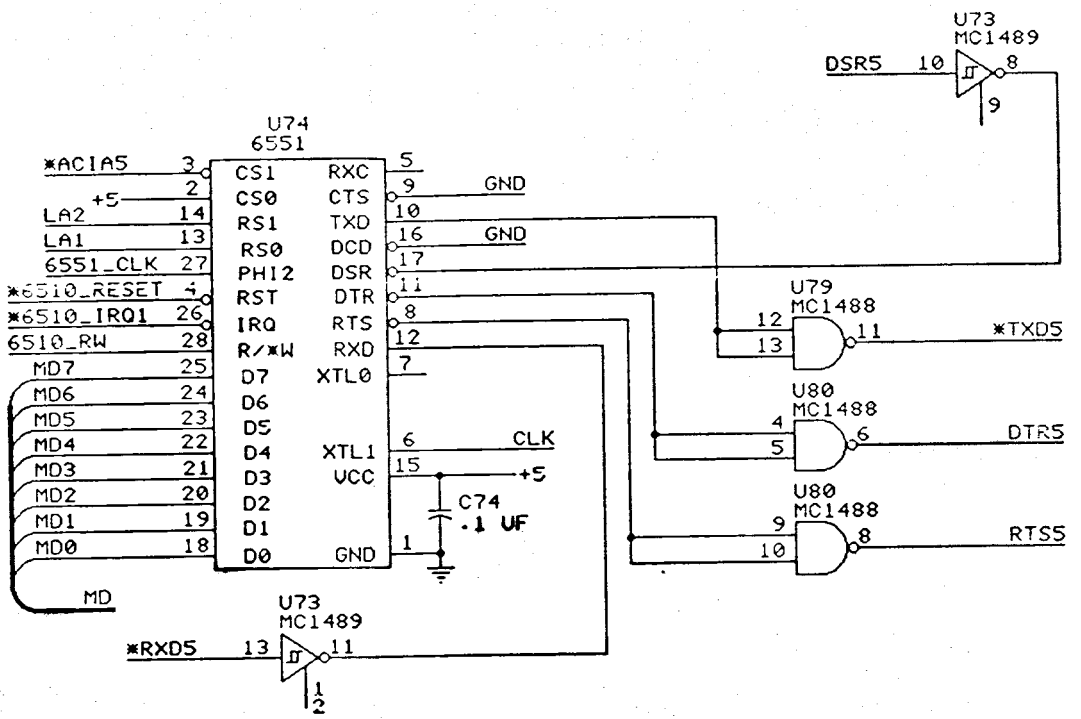
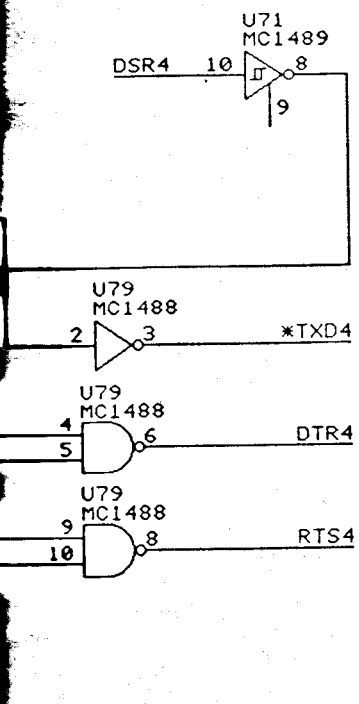
Schematic #312861, Rev. A
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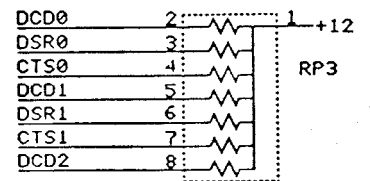
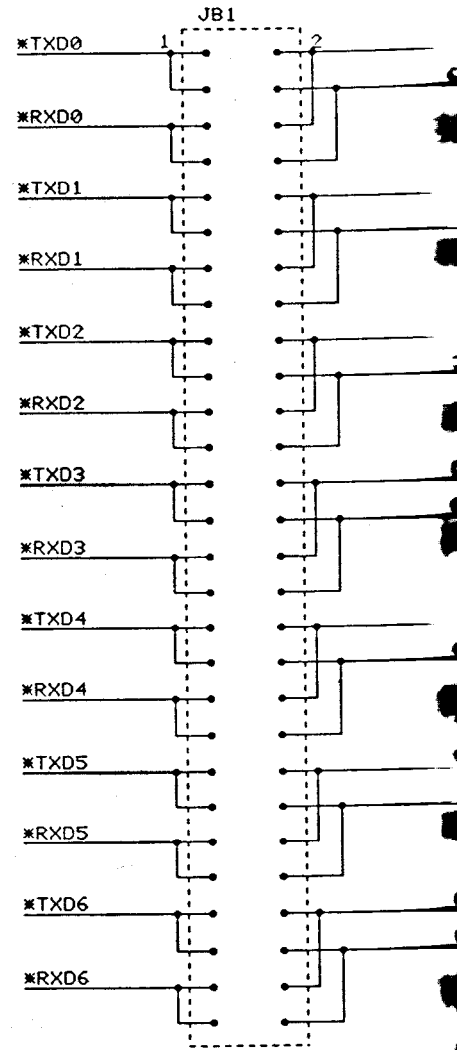


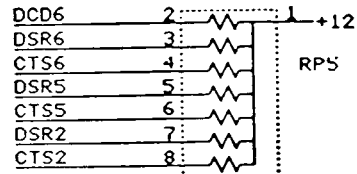
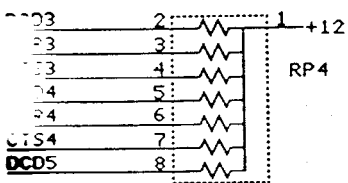
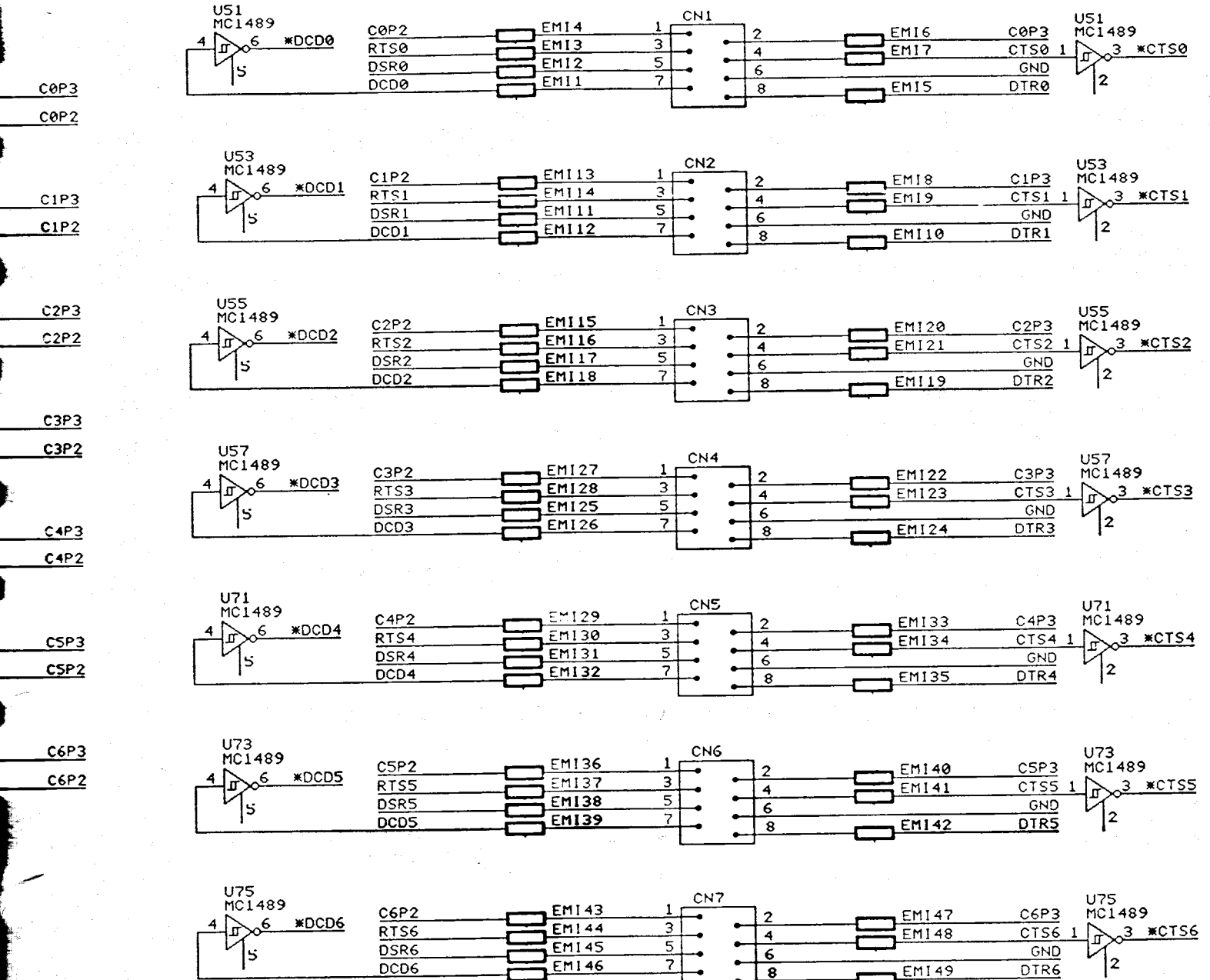
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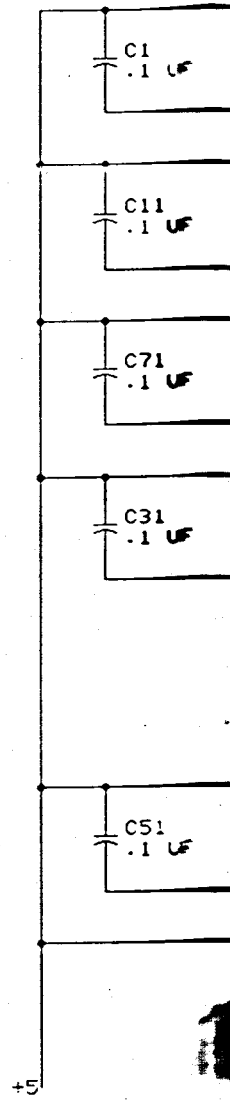


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